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Model 922-DSLH

DSL Hybrid Gateway

User Manual

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Reference Documents

Document Number	Document Title and Description
922-2014-00	DSLH Configuration Drawing
922-0414-00	Model 922-DSL GUI
922-0604-00	922 Remote Firmware Update Guide

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ACRONYMS AND ABBREVIATIONS

BER	Bit Error Rate
DHCP	Dynamic Host Configuration Protocol
DSL	Digital Subscriber Line
EEPROM	Electrically Erasable Programmable Read-Only Memory
GUI	Graphical User Interface
IC	Integrated Circuit
ICMP	Internet Control Message Protocol
IP	Internet Protocol
IGMP	Internet Group Management Protocol
IWIS	Intelligent Well Interface Standardisation
LED	Light Emitting Diode
MAC	Media Access Control (Ethernet)
MIB	Management Information Base
MTBF	Mean Time between Failures
OEM	Original Equipment Manufacturer
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
PLC	Programmable Logic Controller
PLM	Power Line Modem
PPP	Point-to-Point Protocol
PRBS	Pseudo-Random Bit Sequence
QoS	Quality of Service
RSTP	Rapid Spanning Tree Protocol
RTU	Remote Terminal Unit
SCM	Subsea Control Module
SEM	Subsea Electronics Module
SELV	Safety Extra Low Voltage
SHDSL	Symmetrical High-Speed Digital Subscriber Line
SMT	Surface Mount Technology
STP	Spanning-Tree Protocol or Shielded Twisted Pair (cable)
TCP	Transmission Control Protocol
TTL	Transistor-Transistor Logic
uC	Microcontroller
UDP	User Datagram Protocol
VLAN	Virtual Local Area Network

1.0 Introduction

The Model 922-DSLH is a combined (hybrid) Digital Subscriber Line (DSL) modem, optical modem, Ethernet switch, and serial server. As a modem, it offers redundant long range communications over copper and up to 200 km of optical fiber. With the on-board Ethernet switch and a configurable serial server, this highly integrated and multi-functional gateway card incorporates well into Subsea Electronics Modules (SEM) and other types of subsea nodes, often replacing several cards with one board to save space and minimize sparing costs. An optional interface module enables the DSL to run over existing AC power lines.

Supported communication formats include SIIS Level 3 Ethernet and serial protocols such as RS-232, RS-485 and RS-422 (IWIS). The card also performs format conversion, such as Modbus RTU (serial) to Modbus TCP (Ethernet). System integrators can easily adapt legacy serial sensor interfaces to Ethernet based systems with both fiber-optic and high-speed copper communication links. Conversely, Ethernet traffic can now be extended over existing low-speed serial communication links using PPP (Point to Point Protocol).

The Model 922 software provides advanced diagnostics via Modbus TCP for real-time health monitoring of the system as well as easy configuration of all interfaces and modes of operation.

Figure 1-1: Model 922-DSLH Card

The following features and processes are used to ensure reliability is maximized:

- Conductive cooling and detailed thermal analysis
- Advanced diagnostics and health monitoring via Modbus TCP
- Use of industrial temperature range electronic components
- No fuses, electrolytic or tantalum capacitors
- Environmental stress screening
- Full qualification testing
- Traceable components
- Use of field-proven electrical components
- Design for vibration, shock and EMC
- Compatibility with key performance requirements of ISO 13628-6 and API 17F:2014

1.1 Safety Precautions

The following safety precautions should be observed before using this product.

This product is intended for use by qualified personnel who recognize shock hazards and are familiar with safety precautions required to avoid possible injury. Do not make module connections unless qualified to do so.

Before connecting this product to the power source, verify that the output voltage is within the specifications of the product's power supply.

Do not attempt to modify or repair any circuit unless recommended by the manufacturer.

Protect the power cable from being walked on or pinched by items placed or against them.

Always unplug the power cable at the plug, do not pull on the cord itself.

Do not block any ventilation openings.

Do not look into the end of a fiber when it is plugged into a transceiver or active fiber, especially when using a magnifying instrument, such as a fiber microscope.

Handle optical fiber with extreme care. Glass fiber is subject to breakage if mishandled.

2.0 Specifications

Table 2-1: Specifications

Long Range DSL Interface	
No. Ports	1 (via M80 connector)
Protocol	SHDSL Bidirectional over a single twisted pair
Baud Rate	64 kb/s to 15 Mb/s
Cable Length	6.5 km max. (21,325 feet)
Protection	ESD ±15 kV air, ±8 kV contact 500 Vrms isolation
Options	Power line interface (AC power)
Serial Interfaces	
No. Ports	2 (via DIN connector)
Protocol	RS-232, RS-422 (IWIS), RS-485 Software configurable
Baud Rate	230.4 kb/s max., NRZ
Protection	Over-voltage up to ±25 V ESD ±15 kV air, ±8 kV contact 500 Vrms isolation
Ethernet Interfaces (SIIS Level 3)	
No. Ports	2 x Copper (via DIN connector) 1 x Optical (via SFP cage)
Protocol	10/100Base-T(X), copper 100Base-FX, optical
Protection	ESD and transient suppressors (TVS) 500 Vrms isolation
Gateway Modes	Serial (RS-232/485/422) to Ethernet (UDP) PPP server and client Modbus RTU-TCP conversion
Ethernet Switch Layer 2 Functions	Includes broadcast storm protection, rate limiting, flow control, 802.1q VLAN, 802.1p port priority, port mirroring, fast aging
IP Configuration	DHCP with configurable static IP fallback
Diagnostics and Control	Modbus TCP, Webserver, CLI, Telnet
Diagnostics and Control Parameters	Includes temperature, humidity, voltage, current draw, optical power (Tx/Rx), on time and power off events, Ethernet port status/configuration, MIB counters, DSL port status/configuration, DSL SNR, card mftr. data (s/n, p/n, F/W revision)
Redundancy	Automatic link failover (fiber, DSL)*

*Hardware support only

Optical[1]	
Wavelengths	1310 nm and 1550 nm standard CWDM wavelengths (e.g. 1471 to 1611 nm)
Optical Power Budget	20 to 45 dB, depending on SFP installed
Range	10 to 200 km, depending on SFP installed
Options	Bidirectional (single fiber) transceivers
[1] See Subsea Qualified SFP Modules datasheet for available optical transceivers.	
Connectors	
Rear Card Edge	1 x 96-pin DIN 41612 (Ethernet, serial, power)
Front Card Edge	1 x 4-pin Harwin M80 (DSL) 1 x SFP (Ethernet/optical), single or dual LC
Power	
Consumption	5 W typical (8 W max.)
Operating Voltage	+20 to +28 VDC, regulated input
Rated Current	0.4 A max.
Protection	ESD, EMI, over-voltage, reverse voltage, overcurrent (no fuses), 500 Vrms isolation
Mechanical	
Dimensions	3U Eurocard, 4 HP, 160 mm x 100 mm
Mounting	3U Eurocard rack or M2.5 hardware
Options	Front panel
Reliability	
Design Life	> 20 years @ +40 °C
MTBF	> 250,000 hrs @ +40 °C
Testing	Factory Acceptance Test (FAT) At Tmin and Tmax design temperatures
Qualification	ISO 13628-6, API 17F (Q1 Levels) Includes 30 g shock, 5 g vibration
Firmware Update	Failsafe remote firmware update
Options	Environmental Stress Screening (ESS) Custom qualifications per OEM specification
Environmental	
Temperature	-18 °C to +70 °C (design and operation) -40 °C to +85 °C (storage)
Humidity	5 % to 85 % RH, non-condensing

3.0 Architecture Overview

The Model 922-DSLH provides access to one (1) DSL (with or without power line interface board) channel, two (2) RS-232/422/485 isolated serial data channels, two (2) 10/100Base-T(X) Ethernet ports (CU1-2) via a backplane and one (1) SFP (100Base-FX or 10/100Base-T(X)) as shown in the figure below.

The 922-DSLH PCB has a Eurocard form factor with two daughter cards. One daughter card provides the DSL function and the other daughter card (located at the front of the card) provides a power line interface. The copper Ethernet ports CU1, CU2 and serial channels 1-2 are accessed via the 96-pin DIN backplane connector, and the SFP port (located at the front of the card) is accessed via an SFP transceiver.

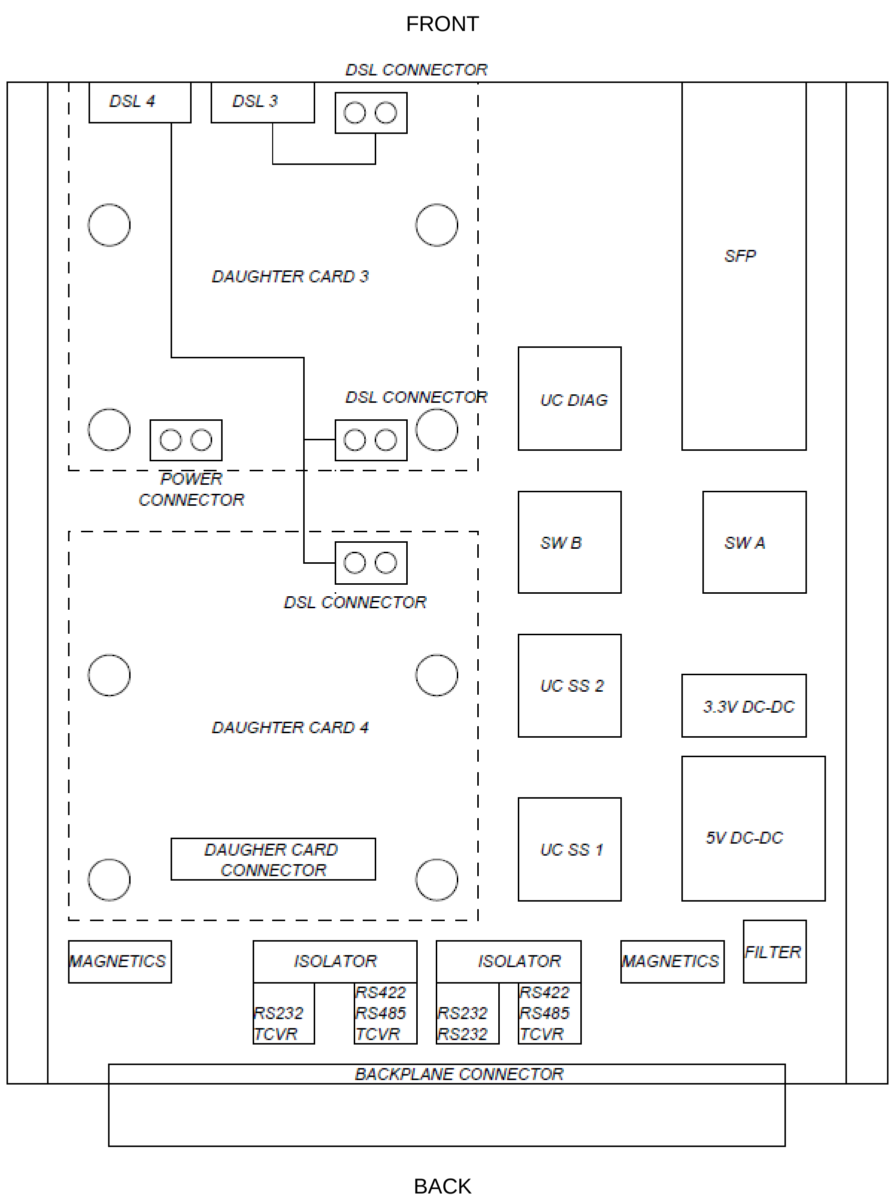

Figure 3-1: Model 922-DSLH Block diagram and Ports

The 922-DSLH includes two Ethernet switches with five (5) internal ports each (P1-P5). The port connections of switches A and B is shown in the table below.

Table 3-1: Ethernet Switch Internal Port Connections

Switch	Port	Connected To	Connection Type
SWA	P1	SWB[P5]	Internal
	P2	Backplane CU1	External
	P3	Serial Server CH1 (uC-1)	Internal
	P4	Not Connected	N/A
	P5	Diagnostics (uC-DIAG)	Internal
SWB	P1	Serial Server CH2 (uC-2)	Internal
	P2	Backplane CU2	External
	P3	SFP	External
	P4	DSL Daughter Card	Internal
	P5	SWA[P1]	Internal

In general, connection types shown as “Internal” should not be changed from the default factory configuration. Connection types shown as “External” (CU1-2 and SFP) might be changed by the user as required to accommodate system-specific requirements. The user must ensure that any switch configuration changes are valid BEFORE saving it in EEPROM and that communications through all ports is as expected after configuration.

3.1 DSL and PLM

The Digital Subscriber Line (DSL) used in the 922-DSLH design is the Symmetrical High-speed Digital Subscriber Line (SHDSL). This SHDSL signaling uses a base band transmission scheme with equal transmit and receive data rates over a single pair of wires. SHDSL supports twisted or untwisted wire pairs. For the remainder of the document, SHDSL will simply be referred to as DSL.

To pass the DSL communications on the same wire as 50/60 Hz AC power, the Power Line Module (PLM) must be used as well as a power line filter. This PLM couples, with capacitors, the DSL signal onto the power line cable and blocks the AC power 50/60 Hz signal from affecting the DSL circuit. In addition to the PLM the AC noise and harmonics need to be isolated from the DSL link. In most cases all that is needed to give this isolation are inductors (3.3 mH) as shown in the figure below. Inductors are needed at both the AC source and the AC load as shown. Since most systems will specify different amperage levels and the power line noise levels may be different, the power line inductor requirements could be custom for each setup.

The figure below shows a typical DSL setup using the 922-DSLH cards. Note that one card is configured as console (STU-C) and the other card is configure as remote (STU-R). The card configuration is done via an Ethernet connection to the card using the sample GUI. Note that the as-shipped factory default configuration is STU-C.

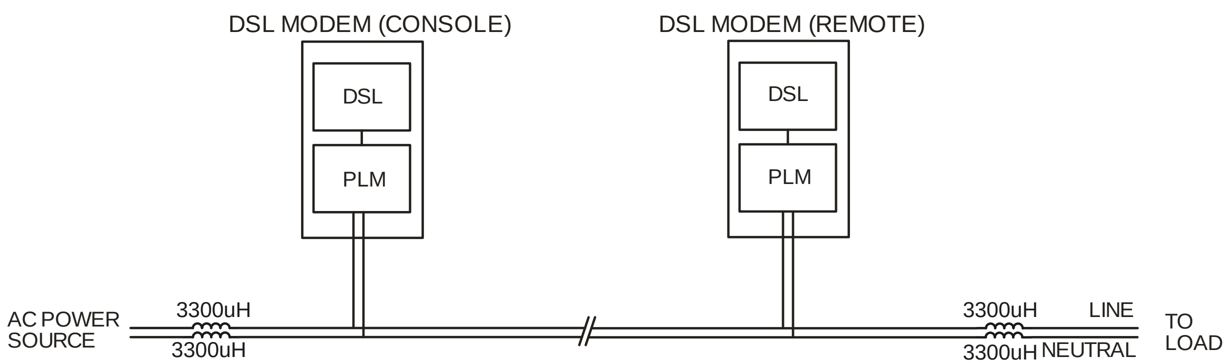

Figure 3-2: Typical DSL Setup

The DSL daughter card acts as a media converter and converts Ethernet to DSL and DSL to Ethernet. The Ethernet communication link can operate at 10 or 100 Mbps and the DSL communication link can operate between 64 Kbps to 15296 Kbps. The DSL daughter card has limited data storage; therefore, the data throughput on the Ethernet link should be controlled (flow control) to ensure that it does not exceed the throughput of the DSL link speed; otherwise data will be lost. The Ethernet and DSL speeds are controlled through the diagnostics GUI (P/N: 922-0414-00).

On power up of the 922-DSLH board the DSL daughter card will attempt to link to a connected DSL interface. Link negotiation may take 1 to 2 minutes before completion, at which point data traffic can start.

The DSL configuration options and bit rates available are shown in the table below.

Table 3-2: DSL Configuration Options and Bit Rates

<table>
<tr><th>Ratemode</th><th>PAM</th><th>Bit Rate (Kbps)</th></tr>
<tr><td rowspan="6">G.SHDSL</td><td rowspan="6">16</td><td>192</td></tr>
<tr><td>384</td></tr>
<tr><td>512</td></tr>
<tr><td>768</td></tr>
<tr><td>1536</td></tr>
<tr><td>2048</td></tr>
<tr><td rowspan="11">G.SHDSL.BIS</td><td rowspan="8">16</td><td>192</td></tr>
<tr><td>384</td></tr>
<tr><td>512</td></tr>
<tr><td>768</td></tr>
<tr><td>1536</td></tr>
<tr><td>2048</td></tr>
<tr><td>2312</td></tr>
<tr><td>5696</td></tr>
<tr><td rowspan="3">32</td><td>2304</td></tr>
<tr><td>3070</td></tr>
<tr><td>5696</td></tr>
<tr><td rowspan="11">Extended</td><td rowspan="5">4</td><td>64</td></tr>
<tr><td>192</td></tr>
<tr><td>1024</td></tr>
<tr><td>2048</td></tr>
<tr><td>2496</td></tr>
<tr><td rowspan="2">8</td><td>192</td></tr>
<tr><td>5056</td></tr>
<tr><td>16</td><td>7616</td></tr>
<tr><td>32</td><td>10176</td></tr>
<tr><td>64</td><td>12736</td></tr>
<tr><td>128</td><td>15296</td></tr>
</table>

Note: Factory default configuration is shown shaded in the table above.

3.2 Ethernet

The DSLH card acts as a SIIS layer 2 managed Ethernet switch. Two copper Ethernet ports CU1 and CU2 are accessed via the backplane 96-pin connector and the third Ethernet port is accessed via the installed SFP (optical or copper depending on the type of SFP installed). Ethernet configuration options are typically performed through the diagnostic GUI.

Table 3-3: Default "As shipped" Ethernet configuration

Parameter	Description
DHCP IP	DHCP is enabled with a 60 second timeout. Default static IP is 192.168.0.100
BP_CU1	Backplane Copper Port CU1 Auto Negotiation, 10/100 Base-T(x), Full Duplex
BP_CU2	Backplane Copper Port CU2 Auto Negotiation, 10/100 Base-T(x), Full Duplex
SFP	100 Base-FX, Full Duplex

3.3 Serial

The DSLH card provides access to two serial ports. Each serial port supports RS-232, RS-485 or RS-422 protocols and are software configurable. The 120 ohm termination for the RS-485 interface can be enabled/disabled via software and by default the termination is disabled.

The DSLH has two dedicated microcontrollers (uC1-2) to provide an Ethernet-to-serial gateway and each uC can be configured in one of four modes: UDP gateway, Modbus gateway, PPP or disabled. All microcontrollers on the card support in field firmware upgrades which can be performed via the sample GUI software.

Table 3-4: Default "As shipped" Serial configuration

Name	Parameter		Default Setting
Serial Channels 1-2 (software)			
Termination	On-board 120 ohm Terminator Enabled / Disabled		120 ohm terminator disabled. (RS-485 or RS-422)
uC1-2 (software settings)			
Network	Static IP address		**uC** / **IP Address** 1 / 192.168.0.201 2 / 192.168.0.202
	Subnet		255.255.255.0
Operational Mode	(A) UDP Gateway. (B) Modbus Gateway. (C) PPP. (D) Disabled.	See Section 3.3.1, **step 3** for possible settings	Option D (disabled) User must configure each serial port.
Serial	Baud Rate Data Bits Stop Bits Parity Flow Control Interface	See Section 3.3.1, **step 4** for possible settings	Baud Rate (baud): 115,200 Data Bits: 8 Stop Bits: 1 Parity: None Flow Control: None Interface: RS-232

3.3.1 Initial User Setup (Serial Ports)

The 922-DSLH mode of operation is determined by the end user. The following steps must be followed during the initial setup of the card.

1. Establish an Ethernet connection between your PC and the card under configuration using the provided sample GUI (922-0414-00). The default uC DIAG IP address is 192.168.0.100. Any of the Ethernet ports (CU1-CU2) can be used to connect to a PC.
   Note: DHCP is enabled by default and connection to the card can take several seconds. This setting can be changed via the Telnet interface.

2. Select serial channel 1.

3. Select the operational mode.
   a. UDP Gateway
      i. Local port: User-defined
      ii. Destination IP: User-defined
      iii. Destination Port: User-defined
      iv. Inter-frame Delay (ms): 2 ms (default). Range: 2 ms ~ 30 sec.

   b. Modbus Gateway
      i. Local port: **502** (default)
      ii. Destination IP: User-defined
      iii. Destination Port: **502** (default)
      iv. RTU Master/Slave: Slave (default, the device connected to the 922 serial channel is an RTU slave)

   c. PPP
      PPP-Client
      i. Password Enabled/Disabled: Disabled (default)
      ii. Username: User-defined (<=8 ASCII characters)
      iii. Password: User-defined (<=8 ASCII characters)

      PPP-Server
      i. Password Enabled/Disabled: Disabled (default)
      ii. Username: User-defined (<=8 ASCII characters)
      iii. Password: User-defined (<=8 ASCII characters)
      iv. Server IP: User-defined
      v. Client IP: User-defined
      vi. Netmask: User-defined

4. Configure the serial port settings
   a. Baud Rate (baud):

110	300	600	1,200	2,400	4,800
9,600	19,200	38,400	57,600	115,200	230,400

   b. Data Bits: 8 or 7* (*=only available in UDP Gateway mode)
   c. Stop Bits: 1, 1.5** or 2 (**=not available in Modbus Gateway mode)
   d. Parity: Even, Odd, Space**, Mark** or None (**=not available in Modbus Gateway mode)
   e. Flow Control: ✓=Supported ✗=Not Supported

Flow Control / Operational Mode	UDP Gateway	Modbus Gateway	PPP
Hardware	✓	✗	✓
Software	✓	✗	✗

   f. Interface: RS-232, RS-422 or RS-485
   g. 120Ω Termination*: Enabled or Disabled (*=not available in RS-232)

5. If required, change the static IP address and netmask.

6. Save configuration.

7. Repeat steps 3-6 for serial channel 2.

8. Trigger a software reset of each channel for the changes to take effect. This can also be achieved by power cycling the card.

9. Done!

4.0 Hardware

The 922-DSLH board can be ordered using the card part numbers shown in the table below.

Table 4-1: Card Ordering Part Numbers

Ordering P/N	Description	Configuration Drawing
922-5016-00	DSL Hybrid Gateway Board, Eurocard	922-2014-00

The 922-5016-00 includes 1x 922-0214-00 Eurocard carrier assembly, 1x 922-0213-00 DSL daughter card assembly and 1x 922-0212-00 PLM daughter card assembly.

The carrier PCBA is a standard 3U Eurocard form factor of 100 mm x 160 mm. This card assembly is suitable for installation in an 8 HP wide (1.6" or 40.64 mm) Eurocard slot if using the 96-pin DIN connector and 8 HP front plate. The backplane DIN connector provides the interface for power, two copper Ethernet ports and two serial data ports. Please refer to the configuration drawing 922-2014-00 for more details.

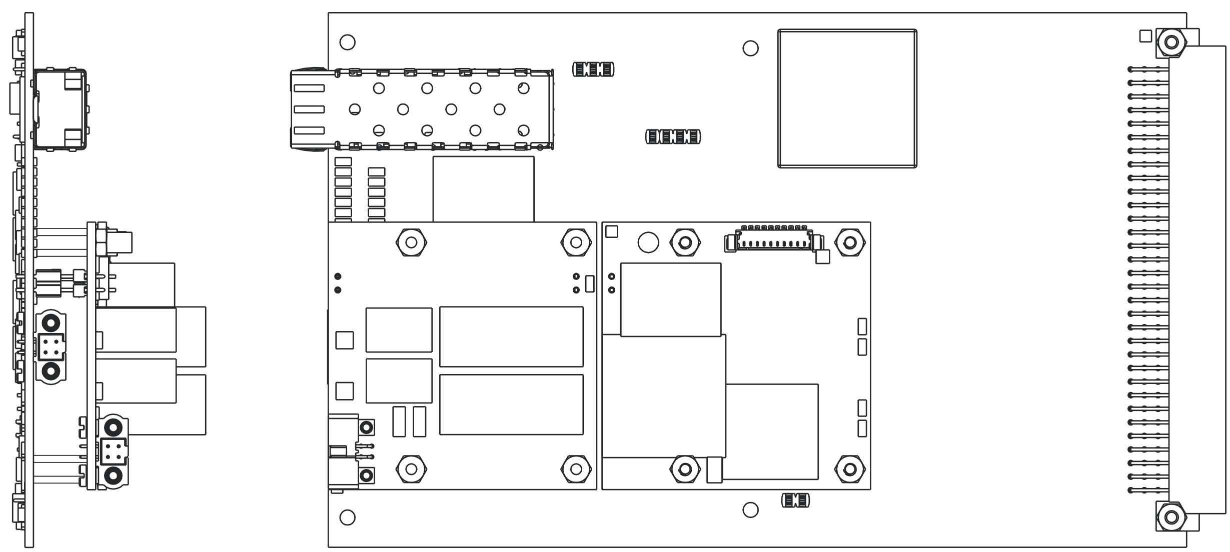

Figure 4-1: Model 922-DSLH PCBA

4.1 General Board Handling

The Model 922 PCBA does not require forced air convective cooling. Generally heat from the card is conducted through the mounting hardware, such as metal standoffs and via the 96 pin backplane connector.

Care must always be taken during the handling of PCBAs to ensure product integrity. The following guidelines should be adhered to in working with PCBAs:

- Always handle boards by the edges and do not touch any connectors or gold tabs.
- Handle boards at an ESD safe workstation with a clean surface.
- Never stack PCB assemblies on top of one another.
- Do not flex boards during handling or when mounted. The mounting surface needs to be flat and even such that the board is not flexed when bolted down.
- Do not cause unnecessary shock and vibration, such as dropping or rough handling of the boards.

5.0 Electrical Connectors and Pin Descriptions

The DSL+PLM connector and Ethernet (SFP) port are located at the front edge of the card. The Ethernet, serial data and power interface is via the 96-pin DIN 41612 connector on the back edge. To interface directly to the DSL daughter card (bypassing the PLM daughter card) contact the factory.

When installing mating connectors to the 4 pin connectors (for DSL+PLM) on the front edge, both mounting screws need to be tightened simultaneously to prevent side loading and possible damage to the connectors.

Table 5-1: Connector/Mating Connector Part Numbers

Ref	Description	Manufacturer	Manufacturer Part Number	Mating Manufacturer Part Number
J3, DAUGHTER CARD	4 –PIN DATAMATE J-TEK CONNECTOR	HARWIN	M80-5400442	M80-4610405
J3, CARRIER CARD	4 –PIN DATAMATE J-TEK CONNECTOR	HARWIN	M80-5400442	M80-4610405
J11, CARRIER CARD	96 PIN DIN41612 CONNECTOR	HARTING	0903-196-6921	0903-296-6824

5.1 Carrier Card with Daughter Cards

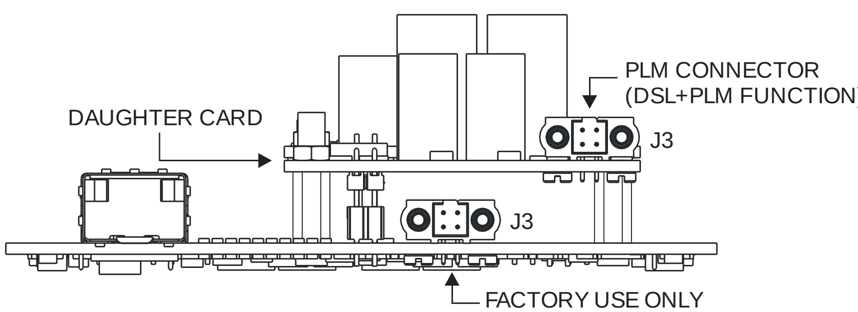

Figure 5-1: Carrier Card with Daughter Cards (Front View)

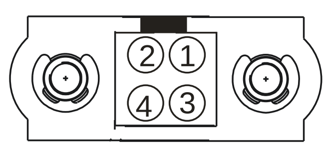

Table 5-2: 4-Pin DSL + PLM Connector Pin-out

Connector Pin Number	DSL+PLM Connector Daughter Card 1 J3, DSL+PLM
1	TIP_PLM1
2	RING_PLM1
3	CHASSIS
4	CHASSIS

5.2 96-pin DIN 41612 Backplane Connector (J11)

Figure 5-2: DIN 41612 (96-pin) Backplane Connector (Front View)

Table 5-3: DIN 41612 (96-pin) Backplane Connector Pin-out

Pin	Name		
	Row A	Row B	Row C
1	TXP_CU1	REF_CU1	RXP_CU1
2	TXM_CU1	REF_CU1	RXM_CU1
3	NC	NC	NC
4	NC	NC	NC
5	NC	NC	NC
6	NC	NC	NC
7	VIN1+	VIN1+	VIN1+
8	VIN2+	VIN2+	VIN2+
9	NC	NC	NC
10	VIN-	VIN-	VIN-
11	VIN-	VIN-	VIN-
12	NC	NC	NC
13	UC1_TX+	UC1_RX+	UC1_ISO_GND
14	UC1_TX-	UC1_RX-	NC
15	UC1_RTS	UC1_CTS	NC
16	UC1_TX232	UC1_RX232	UC1_ISO_GND
17	UC2_TX+	UC2_RX+	UC2_ISO_GND
18	UC2_TX-	UC2_RX-	NC
19	UC2_RTS	UC2_CTS	NC
20	UC2_TX232	UC2_RX232	UC2_ISO_GND
21	NC	NC	NC
22	NC	NC	NC
23	NC	NC	NC
24	NC	NC	NC
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	TXP_CU2	RXP_CU2	REF_CU2
30	NC	NC	NC
31	TXM_CU2	RXM_CU2	REF_CU2
32	NC	NC	NC

NC = No Connect

5.3 Part Locations and Diagnostic LEDs

Refer to the figures below for location of connectors, hard wire jumper and on-board diagnostic LEDs on the card. Note some factory testing headers and jumpers may not be exactly as shown depending on the PCB revision.

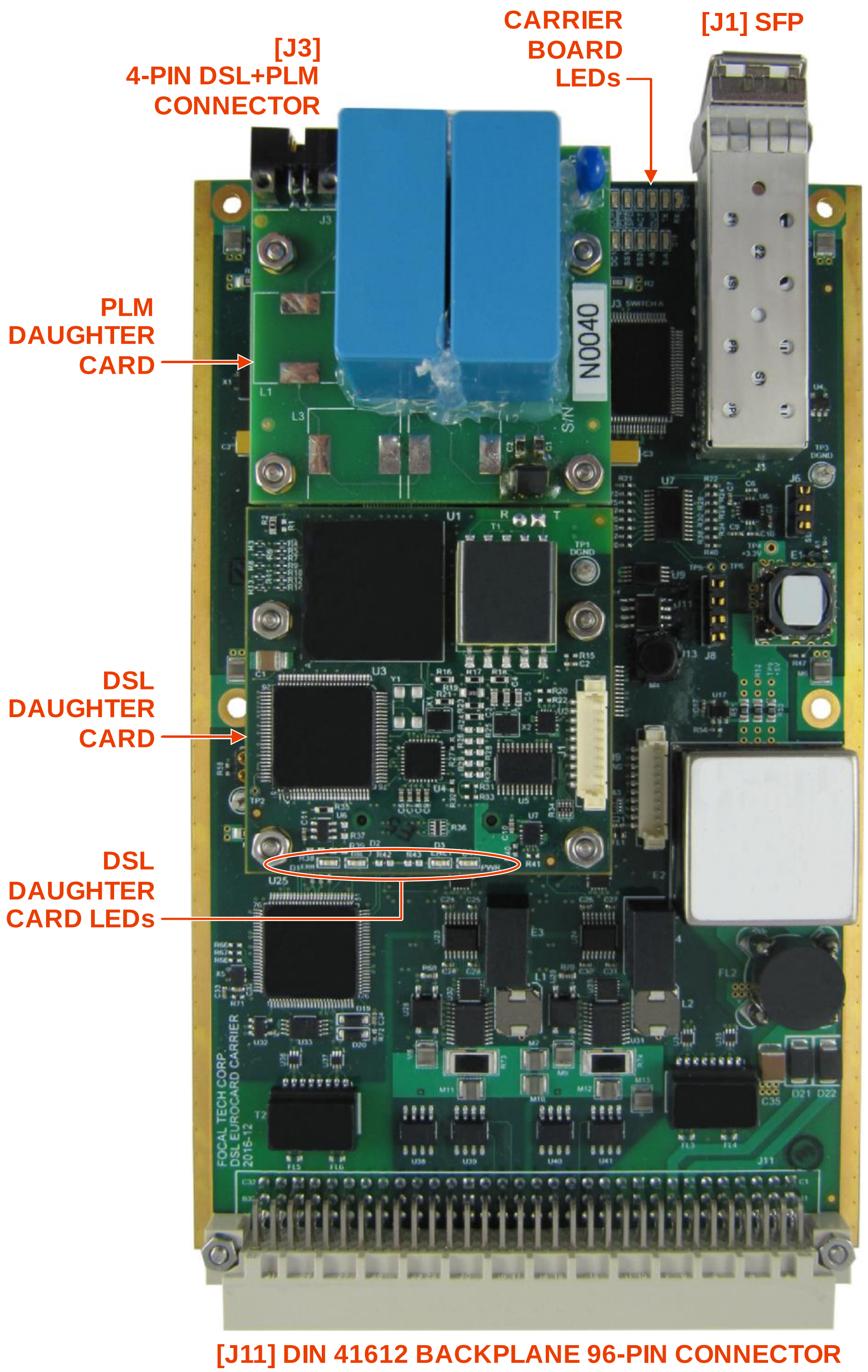

Figure 5-3: Model 922-DSLH Part Locations (Top View)

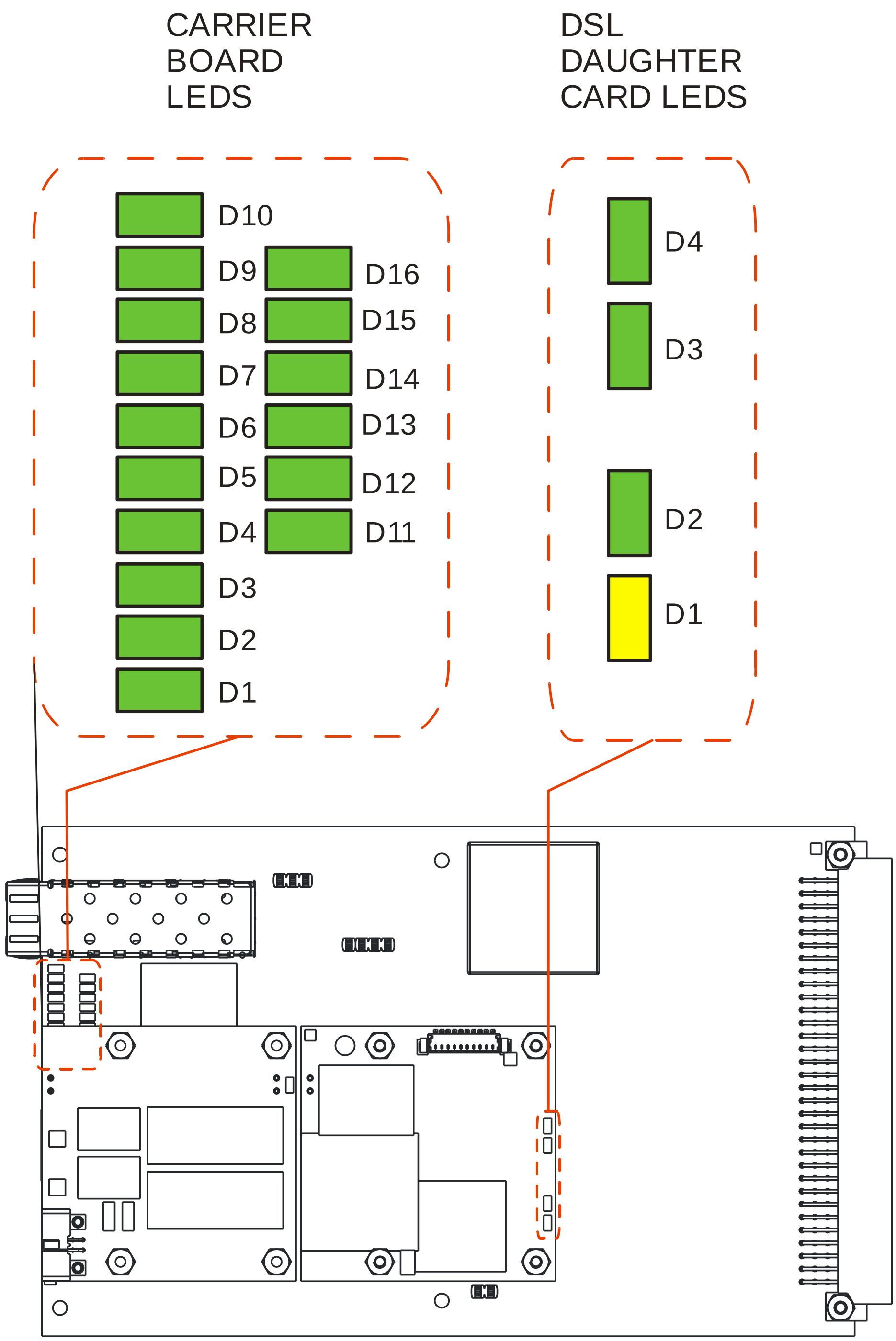

Figure 5-4: LED Locations

Table 5-4: Carrier Board Diagnostic LEDs

Reference Designator	Name	Description
D1	DSL FAULT	*Factory use LED.*
D2	DSL LINK	OFF = No DSL Link. ON = DSL Link Up (initialization completed successfully).
D3	CU1 SPD	*Ethernet Speed CU1:* ON = Linked at 100Base-Tx. OFF = Linked at 10Base-T.
D4	CU1 ACT	*Ethernet Link/Activity CU1:* OFF = No Link. Solid ON = It indicates there is a link for 10Base-T or 100Base-TX, but no data is being transmitted or received. Blinking = It indicates data is being transmitted or received for either 10Base-T or 100Base-TX.
D5	CU1 DUP	*Ethernet Duplex Mode CU1:* ON = Full Duplex. OFF = Half Duplex.
D6	CU2 SPD	*Ethernet Speed CU2:* ON = Linked at 100Base-Tx. OFF = Linked at 10Base-T.
D7	CU2 ACT	*Ethernet Link/Activity CU2:* OFF = No Link. Solid ON = It indicates there is a link for 10Base-T or 100Base-TX, but no data is being transmitted or received. Blinking = It indicates data is being transmitted or received for either 10Base-T or 100Base-TX.
D8	CU2 DUP	*Ethernet Duplex Mode CU2:* ON = Full Duplex. OFF = Half Duplex.
D9	SFP LINK	ON = Optical link good. OFF = No optical link.
D10	SFP LOS	ON = SFP RX power low. OFF = SFP RX power good.
D11	PWR	ON = Power Good (card is on). OFF = Card is Off.
D12	DC1	*DSL and on-board Ethernet switch link:* OFF = No Link. Solid ON = Internal Ethernet link between DSL daughter card and Ethernet switch. Blinking = Ethernet TX/RX Activity. Note: Normally this LED is ON or blinking when a DSL daughter card is installed.
D13	SS1 ACT	OFF = No Link. Solid ON = Internal Ethernet link between Serial Server CH1 and Ethernet switch. Blinking = Ethernet TX/RX Activity. Note: Normally this LED is ON or blinking.
D14	SS2 ACT	OFF = No Link. Solid ON = Internal Ethernet link between Serial Server CH2 and Ethernet switch. Blinking = Ethernet TX/RX Activity. Note: Normally this LED is ON or blinking.
D15	A-B ACT	OFF = No Link. Solid ON = Internal Ethernet link between SWA and SWB. Blinking = Ethernet TX/RX Activity. Note: Normally this LED is ON or blinking.
D16	B-A ACT	OFF = No Link. Solid ON = Internal Ethernet link between SWB and SWA Blinking = Ethernet TX/RX Activity. Note: Normally this LED is ON or blinking.

Notes:
1. LEDs in the table above are green color when on.
2. LEDs are valid for cards with uc DAIG FW version >= 0xA4.

Table 5-5: DSL Daughter Card Diagnostic LEDs

Reference Designator	Name	Description
D1	ERR	OFF = Normal operation of the DSL board. ON or BLINKING = An error has occurred. Note: This LED will flash twice (orange) on power-up.
D2	DSL	OFF = The DSL is not active, which is during the power up initialization. BLINKING 1Hz rate = Searching and waiting for DSL link partner. BLINKING 3Hz rate = Link partner detected and initializing a DSL link. Solid ON = DSL link established and ready for DSL data transmission.
D3	ENET	OFF = No Link. Solid ON = Internal Ethernet link between DSL daughter card and on-board Ethernet switch. Blinking = Ethernet TX/RX Activity. Note: Normally this LED is ON or blinking when a DSL daughter card is installed.
D4	PWR	OFF = No +3.3V power on the board. ON = The board is powered with +3.3V.

5.4 Electrical Interfaces

This section shows the schematics of the user accessible interface circuits, which are the +24V power input, copper Ethernet interfaces, and serial channel interfaces.

5.4.1 +24V Power Input

The power input interface schematic in the figure below shows the input protection diodes, common mode EMC filter and DC-DC converter. **Power input must be within +20VDC to +28VDC. Ideal input voltage is +24VDC and provided by a supply with a Safety Extra Low Voltage (SELV) rating.** See section 2.0 for specification details. Power inputs VIN1+/VIN2+ and diodes D21/D22 allow for redundant power supply hookups. The diodes also provide reverse voltage protection. The DC-DC converter provides an electrically isolated +3.3V DC output.

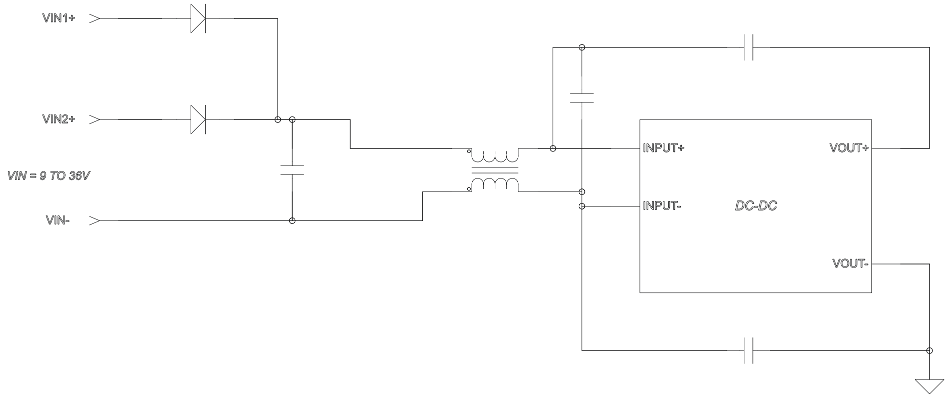

Figure 5-5: Power Input Interface Schematic

5.4.2 Ethernet Interface

The Ethernet interface schematic shown in the figure below, is identical for both Ethernet copper ports. This schematic shows the transformer isolation, ESD protection, REF (shield), and termination used.

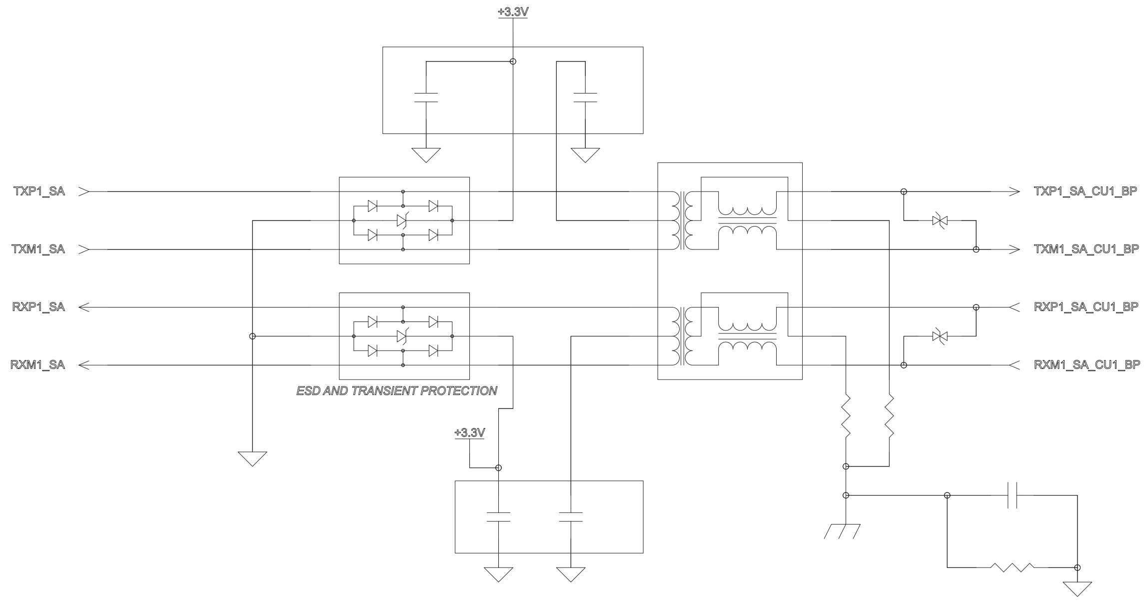

Figure 5-6: Copper Ethernet Interface Schematic

5.4.3 Serial Channel Interface

The serial interface is identical for all serial channels. The card supports software configurable RS-232/422/485 interfaces. The termination for the RS-485 interface can be controlled via software. The serial I/O are protected per IEC-61000-4 for ESD, surge and EFD. See section 2.0 for specification details.

5.4.4 Isolation and Grounding

A “chassis ground” is provided on the printed circuit board for EMC and ESD performance. It is accessible via the four mounting holes at the front, as shown in the figure below, and may be connected to a metal enclosure or mounting plate with appropriate conductive hardware. The two mounting holes at the back of the card are isolated. As the card is not intended for use with primary circuits or other hazardous voltages, the chassis node is a functional earthing point and is not intended as a protective earth (PE) terminal. The mounting holes are thermally connected to the board’s power and ground planes and intended as a means to extract heat from the board.

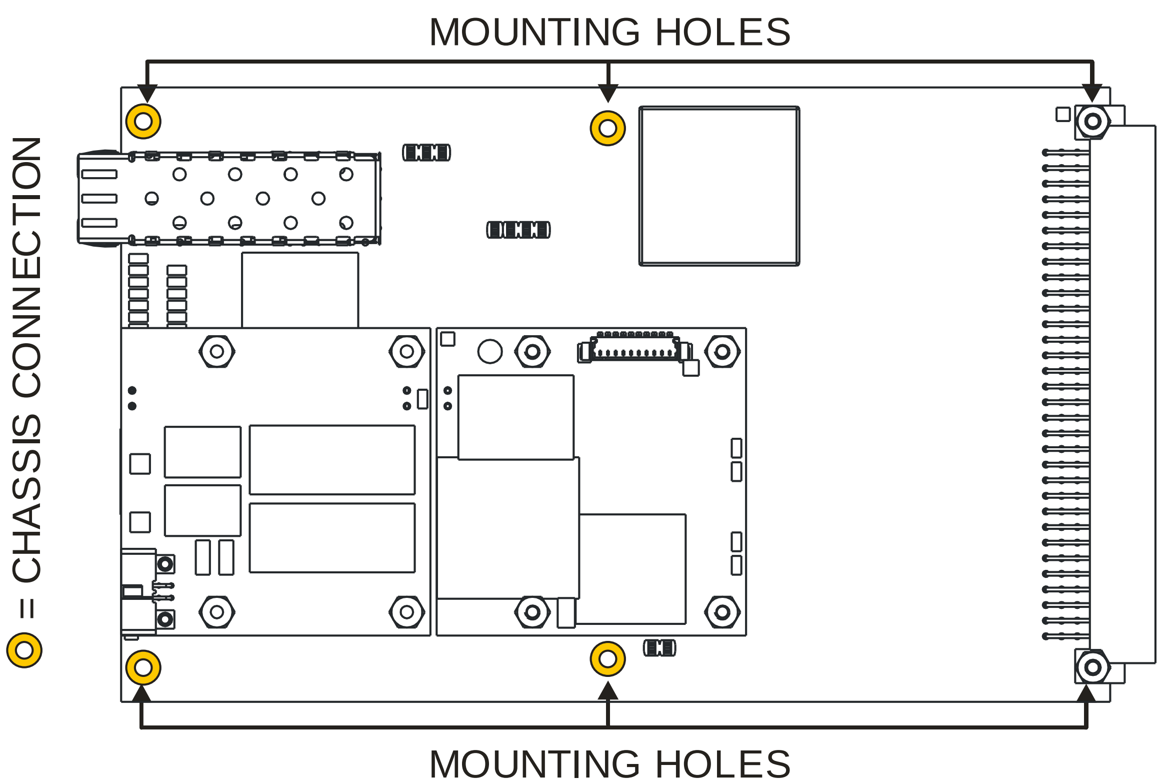

Figure 5-7: Mounting Holes Locations

Reference (REF) lines are provided with each copper port and may be used as shield reference connections for shielded twisted pair (STP) cabling. Typically, unshielded twisted pair (UTP) cabling should be used, such as Cat 5e. If STP cabling is required, shields may need to be terminated and connected to the enclosure entry point. Note that the REF lines are connected to chassis through a parallel capacitor and 10 MΩ bleed resistor.

This card is intended for use with SELV rated power supplies and Ethernet Environment A, as defined by IEEE 802.3 section 27.5.3. Extension of copper Ethernet segments that cross Environment B boundaries may require additional isolation. Note that VIN+ and VIN- are isolated from chassis.

6.0 Optical Interface

6.1 Optical Transceivers

The 922-DSLH card is able to communicate optically using a small form-factor pluggable (SFP) transceiver. The device can be ordered with a wide selection of qualified SFPs, depending on the application distance, optical budget, and fiber count requirements. Depending on the SFPs selected, the card is able to function on one (1) to two (2) fibers. The card supports SFPs with 100 Mb/s. In general, lower optical data rates have higher optical power budget and longer range.

Standard, API qualified, SFPs utilize two separate fibers, typically one transmitting in each direction at 1310 nm for shorter links (< 50 km), or 1550 nm for longer links, up to 200 km at 100 Mb/s.

Bidirectional SFPs, or "Bidis", are available with integrated wavelength division multiplexing (WDM) optical components, providing bidirectional operation using two wavelengths on a single fiber (e.g. 1310/1550 nm). Bidi SFPs are typically limited to a range of 50 km.

SFP transceivers with CWDM wavelengths (1471 nm to 1611 nm) may be used to combine up to four sets of modems (i.e. 8 CWDM wavelengths) on the same fiber. CWDM systems require additional optical modules that may include power splitters, for redundancy, and/or CWDM couplers for combining or separating wavelengths. Optical modules are available from the factory in a variety of packaging options. Note that the combination of multiple wavelengths on a single fiber may cause the combined optical power levels to exceed Class I power limits.

6.2 Optical Fiber

The card communicates using one SFP transceivers per card, which requires up to two fibers. The fiber must be singlemode, such as SMF-28e (9/125 µm) or equivalent. For links over 100 km, dispersion shifted singlemode fiber (SMF-DS), should be considered to minimize dispersion on the 1550 nm wavelength.

Bend-insensitive jumpers with reduced boot-lengths may be used to allow for fiber routing to the card within confined spaces, such as in subsea pressure housings. These jumpers are available from the factory or third party vendors. Regardless of the fiber types used, the following handling guidelines should be followed:

Observe the bend radius of fiber optic cables at all times

When mounting, disassembling, or reassembling the cards, ensure that no fibers are subjected to bends in excess of those held by the natural routing of the fibers. The minimum bend radius of standard singlemode SMF-28e fibers should generally be no less than 25 mm, though single loops may be less than this – as low as 15 mm – without damaging the fibers. Keep in mind that allowable values are dependent on the type of fiber and the environment, and cable manufacturers typically specify the minimum bend radius. Avoid even temporary bends with a radius less than 15 mm, which may induce cracks that affect long-term reliability of the fibers. Use bend insensitive fibers where tight bends are expected during installation or operation.

Ensure fiber optic components are of the same type

All jumpers, cables, connectors, couplers, and Fiber Optic Rotary Joints (FORJs) used in the external optical system connecting the card must use the same type of fiber, i.e. all components in the fiber link should be singlemode. A single mismatched jumper in the system may cause intermittent or persistent optical link errors. Do not rely on cable jacket or connector colors alone to determine the type of optical fiber.

6.3 Optical Budget, Range, and Bit Error Rate (BER)

A variety of approved and tested SFP transceivers are available from Focal Technologies for maximum distances from 10 km to 200 km. The optical power budget is dependent upon the SFPs selected, but typically varies from 16 dB to 45 dB with an optical bit error rate (BER) of 1×10^{-12}. Contact the factory for the current list of available, API qualified transceivers.

Optical receivers will experience errors if the received optical power is too low (i.e. below the receive sensitivity of the photo detector). Ensure the total optical losses of the components in the external cable system (jumpers, cables, connectors, couplers, etc.) are less than the specified optical power budget of the SFP combination used. For detailed measurements or trouble-shooting, a calibrated optical power meter is recommended.

Optical receivers can also saturate and experience errors if the received optical power is too high. This is more likely to occur (especially in a lab environment) when using high power transceivers. Use a 5 or 10 dB fixed attenuator in line with each fiber during bench tests or with short, low loss links to ensure a minimum level of attenuation is present. A variable optical attenuator (VOAT) can be used for simulating system losses or testing the maximum insertion loss supported. In some high power systems, receivers can actually be damaged by excessive optical power, so a fixed attenuator is recommended even when using a VOAT to ensure a minimum attenuation at all times.

Adding attenuators for bench testing simulates only the insertion loss of a field system. Dispersion effects are not simulated with attenuators and should be verified with spools of test fiber matching the length of the system being designed. Dispersion effects con incur a power penalty of 1-2 dB. Please contact the factory for assistance with optical system analysis and recommendations.

6.4 Return Loss Tolerance

The optical system external to the card should have a minimum of 20 dB return loss. Excessive optical reflections may degrade optical budget and/or reduce transceiver lifetime.

For systems with bidirectional optical transmission on a single fiber, sufficient reflected optical power on one wavelength can interfere with received power on another wavelength and cause data errors. Return loss specifications for systems with WDM or CWDM couplers must be determined based on a more detailed analysis of the maximum link attenuation, optical levels, and filter characteristics, but typically 25-30 dB return loss is sufficient to ensure reflected optical power does not cause link errors.

6.5 Optical Power

All optical power levels are within Class I limits (eye-safe), however as general safe practice, fiber connectors should not be held close to the eye for inspection. Note that all of the SFP optical wavelengths used for Model 922 links are infrared and not visible, even at high power levels.

Active optical outputs should NEVER be viewed with a magnifying device of any kind (e.g. fiber microscope).
Always turn off all transmitters before inspecting fibers, optical connectors, or optical bushings.

6.6 Optical Connectors

Optical connectors for the SFPs qualified for use with the 922-DSLH are LC type. The mating connector for the LC interface, with a standard boot, is shown in the figure below. Ruggedized (metal) LC compatible connectors, such as the *Molex LC2+* and *Diamond F3000*, can also be used.

Figure 6-1: LC connector with Standard Boot

Standard SFP optical transceivers typically have a transmit and receive optical bushing (LC type) for dual fiber operation. The transmit side (Tx) and the receiver side (Rx) of an SFP is shown below.

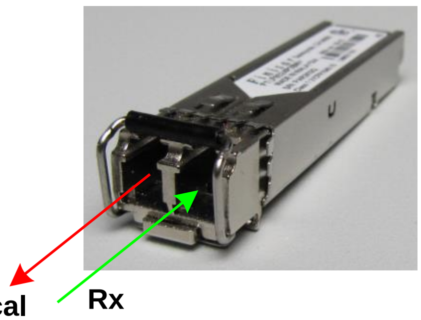

Figure 6-2: Tx and Rx ports of an LC-type SFP Transceiver

Optical Connectors Care:

It is critical to ensure all fiber connectors are clean and free of dirt and debris. Even a small amount of dirt or fluid contaminant may degrade link performance, and most reported optical link problems are due simply to poor or contaminated optical connections.

- Keep protective dust covers on fiber connectors and bushings when not in use.
- Do not touch the white ceramic ferrules of the connectors with bare hands or objects other than cleaning materials.
- Prior to making a fiber connection, clean the barrel and tip of the ferrule using a suitable solvent, such as reagent grade isopropyl alcohol, and a lint-free optics cleaning tissue, such as Kimwipes® EX-L. Carefully dab any dirt or debris off the face of the ceramic ferrules. Excessive dirt may need to be cleared with pressurized air from a can prior to wiping the ferrule to avoid scratching the fiber itself. Do not used air from a compressor as it may be contaminated with oil.
- During mating or un-mating of fiber connectors with bushings, keep the connector aligned as straight as possible. Avoid side loading the ceramic ferrule, which can crack the internal alignment sleeve in the bushing.
- Each fiber connector should be inspected with a handheld fiber microscope prior to final assembly to ensure there are no scratches, pits, debris, or fluid contamination on the fiber face. Ensure connectors do not have any optical power present prior to inspection, e.g. with a handheld power meter.

7.0 Functionality

The main functions of the 922-DSLH card are to provide a bi-directional media conversion between copper Ethernet, copper DSL, and optical data as well as providing two gateways between copper Ethernet and serial data. The Ethernet interface is accessed via the backplane connector and the DSL and optics via the front panel connectors. The network protocols supported by the serial data gateways are UDP, Modbus TCP and PPP. The serial protocols supported are RS-232, RS-422 and RS-485. This gateway functionality is handled by two microcontrollers uC1 and uC2 (one uC per serial channel) and two Ethernet switches (SWA and SWB).

In addition to the media conversion and serial to Ethernet gateways, the 922-DSLH provides, via the microcontroller diagnostic, extensive diagnostics information including but not limited to card S/N, FW version, card temperature, humidity (RH), voltage, current draw, card powered up time, card turn off events, SFP diagnostics (including optical link status and TX/RX power levels), Ethernet copper port link and both DSL link status and user-defined switch configurations. The DSL link configuration and serial gateway configuration can also be controlled via the uC diagnostics.

7.1 Gateway Functionality (uC1-2)

The 922-DSLH is a gateway which provides the conversion between RS-232/422/485 serial data and Ethernet packets. The card can be configured in one of four modes of operation: UDP Gateway, Modbus Gateway, PPP Gateway or disabled (no gateway functionality).

7.1.1 UDP Gateway

Serial to UDP. The RS-232/422/485 serial data is received from the serial port and it is stored into a buffer. When the buffer is full or user specified inter-frame timeout is reached, the gateway sends the data in the buffer as a UDP packet to a user specified destination (configurable IP and UDP port).

UDP to Serial. The UDP packet is received from the card's Ethernet port and the gateway listens to a user specified UDP source (configurable IP and UDP port). If any packet is received on the source, the gateway sends out the data through the corresponding serial port immediately. In this mode, all serial port settings, such as baud rates, flow control, parity, etc., are supported.

7.1.2 Modbus Gateway (Modbus RTU to Modbus TCP)

This mode has two configuration options: RTU slave and RTU master.

RTU Slave. When the gateway is configured to connect a RTU slave on its serial port, it will create a Modbus TCP server and listen to the Modbus TCP port (port 502 by default). Once a TCP client is connected to this port, the gateway will forward all Modbus request from the TCP client to the serial port. It also forwards all responses from the RTU slave to the TCP client.

RTU Master. When the gateway is configured to connect a RTU master on its serial port, it will keep trying to connect to the user specified Modbus TCP server until the connection is successfully made. Once the connection is built, the gateway will forward all Modbus request from the RTU master to the TCP server. It also forwards all responses from the TCP server to the RTU master.

Please note that only one TCP connection is allowed for each gateway. In this mode, flow control is not supported. The support of data bits, stop bits and parity bit complies with Modbus specification.

7.1.3 IWIS PPP Gateway (PPP to IP)

The PPP to IP gateway creates a tunnel which passes Ethernet traffic between a serial device and an Ethernet network. From PPP perspective, users can configure the gateway as either a PPP client or PPP server. When it is configured as a client, its IP address is obtained from its counterpart – the PPP server. When it is configured as a server, users have to specify the local (server) IP address, the remote (client) IP address and its network mask. The current implementation on the 922-DSLH uses the Password Authentication Protocol (PAP) for user authentication. The same user name and password should be used on both sides (the client and the server). In PPP mode, the serial port should NOT be configured using software flow control.

7.2 Network Configuration

7.2.1 MAC Address

Each 922-DSLH card is assigned three (3) unique MAC addresses (one MAC per uC [uC1-2 + uC DIAG]). The MAC address is marked on the bottom side of the board, and recorded at the factory with cross-reference to serial number, and thereby customer and order, should it ever need to be retrieved.

7.2.2 IP Address

Diagnostics (uC DIAG)
The diagnostics IP address (uC DIAG) for the 922-DSLH can be assigned statically via Telnet or dynamically using dynamic host configuration protocol (DHCP). Either mode can be enabled remotely using a virtual Telnet terminal over any Ethernet port, followed by power cycling the board after the changes has been submitted to the card.

By factory default, the card obtains an IP address using DHCP, configured with a 60 second timeout. If the connecting network does not support DHCP to provide the Model 922 with a dynamic IP within 60 seconds, the card will automatically revert to use locally stored (i.e. static) IP address and network settings. Factory default network parameters are shown in Table 3-3: Default “As shipped” Ethernet configuration.

Gateway (uC1-2)
Both gateway microcontrollers have two types of IP addresses. One is the static (local) IP address and the other is the destination IP address. The static IP address of each uC is configured at the factory with default network parameters as shown in Table 3-4: Default “As shipped” Serial configuration. The destination IP address must be set by the end user. Both the static and destination IP addresses can be changed and/or updated using the sample GUI.

7.3 Diagnostics Functionality (uC DIAG)

7.3.1 IP Connectivity

The 922-DSLH can host the following IP connections simultaneously:

- **Up to four (4) Modbus TCP clients over any Ethernet port,** including ‘remotely’ (i.e. from topside card) via one of the Ethernet copper ports. The Modbus TCP connection provides diagnostics information, which can be accessed using Modbus software (e.g. sample Focal GUI). The recommended poll rate for a single TCP client is 1 second. Refer to section 9.8 for more details about multiple TCP clients.

- **One (1) Telnet over any Ethernet port**, including ‘remotely’ via the copper ports. There is a limited set of commands available. Telnet is used primarily for IP address and network setting configuration.

7.4 Diagnostics and Control via Modbus TCP/IP

Modbus TCP protocol is used to provide diagnostics and user control messages via a TCP/IP connection to the 922-DSLH. The Modbus TCP protocol stack is illustrated in the figure below. Local card status and control registers are accessible via Modbus TCP/IP from the topside or other subsea equipment over any Ethernet port.

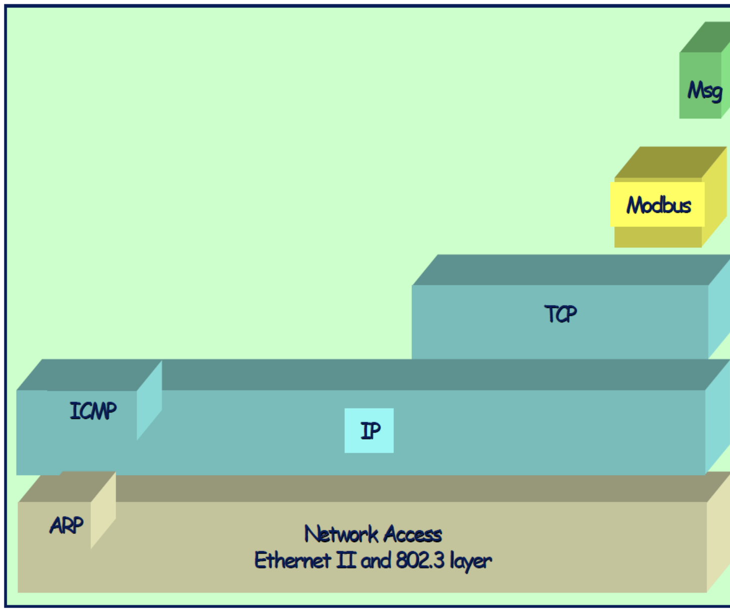

Figure 7-1: Modbus TCP Protocol Stack

7.4.1 Diagnostics and Modem Status

Remotely accessible, real-time diagnostic data and status information is available from the Model 922. This information can be used to determine real-time state of health or to monitor long-term trending of critical parameters to estimate the remaining life of the unit.

Diagnostic and status information is retrieved from the following:

1. On-board microcontroller (uC DIAG). A bank of ADCs is used to monitor board voltage rails. The uC also provides status information such as serial number, MAC address, IP address and other network settings.
2. Onboard sensors including a temperature sensor, humidity sensor, current monitor, and ON time counter.
3. Status of the on board optical transceiver diagnostics (including optical link, transmit and receive optical power levels).
4. Status and configuration of the serial to Ethernet gateway channels.
5. Status of the DSL link such as the DSL Mode, Bitrate, TC-PAM, SNRM and LATN. **Note** that DSL parameters such as Device Mode (STU-C/R), Ratemode, Bit Rate and PAM can also be configured and save it in the card using the sample GUI.
6. Status registers of Ethernet Switch. Key Ethernet status indicators are:
    - Link (speed/duplex) and activity status of copper Ethernet ports
    - Port mirroring/monitoring/sniffing
    - MIB counters for statistical gathering of dropped packets, CRC errors, packet sizes, unicast/multicast, etc.

Diagnostics and status information are retrievable using Modbus TCP over any Ethernet port. Most diagnostic information is available using the Modbus TCP register map, per section 10.0. Limited configuration information is available over the Telnet as described in section 8.0.

Focal™ has created a sample version of a .NET graphical user interface (GUI) for use on Microsoft Windows with a Modbus TCP backend for integration and bench testing the 922-DSLH Modbus functionality. Typically users have or develop their own Modbus TCP interfaces for local PLCs and other controllers. A screenshot of the sample GUI P/N: 922-0414-00 is shown in the figure below.

Figure 7-2: Sample .NET GUI for Modbus TCP Access to 922-DSLH

7.4.2 Control and Configuration Capabilities

The 922-DSLH supports some read/write control registers. Supported control and configuration functionality includes:

- Ethernet Switch port control registers (e.g. forcing speed/duplex, flow control/back pressure, rate limiting, packet aging, multicast protection, port priority, virtual local area network (VLAN) configuration, etc.)
- Triggering load of switch registers from configuration saved in electrically erasable programmable read only memory (EEPROM) (see section 9.2)
- Field update of embedded firmware, and user-controlled switching between stored firmware versions.
- DSL configuration
- Ethernet-serial gateway configuration

7.5 Ethernet Switch Configuration

On power up, the switch operational parameters are immediately configured via pull-up and pull-down resistors. Registers within the two Ethernet switch ICs (switch A and B) can also be user configured over any copper Ethernet port using Modbus TCP to override the default configuration.

On power-up, the Ethernet switches A and B are configured as follows:

- Auto-negotiation with auto MDI/MDI-X on all five user copper ports
- Broadcast frames limited to 0.05% throughput or 4 frames per 50 ms.
- Maximum frame length: 1536 bytes
- Share buffer memory based on port activity
- Priority disabled

The registers shaded in Table 7-1 Error! Reference source not found. **are intended for factory use only and should not be modified. Changing them could disable critical card functions. All other register changes could also affect some of the card functionality. If this occurs accidentally, the switches can be reverted to default condition with a power cycle.**

Table 7-1: Register Map for Ethernet Switches 'A' and 'B' (Factory Use Shaded)

Offset		Description*	
Decimal	**Hex**	**Switch 'A'**	**Switch 'B'**
0-1	0x00-0x01	Chip ID Registers	
2-11	0x02-0x0B	Global Control Registers	
12-15	0x0C-0x0F	Reserved	
16-29	0x10-0x1D	Port 1A (SWA-SWB) Control Registers	Port 1B **(uC2)** Control Registers
30-31	0x1E-0x2F	Port 1A (SWA-SWB) Status Registers	Port 1B **(uC2)** Status Registers
32-45	0x20-0x2D	Port 2A (**CU1**) Control Registers	Port 2B **(CU2)** Control Registers
46-47	0x2E-0x2F	Port 2A (**CU1**) Status Registers	Port 2B **(CU2)** Status Registers
48-61	0x30-0x3D	Port 3A **(uC1)** Control Registers	Port 3B **(SFP)** Control Registers
62-63	0x3D-0x3F	Port 3A **(uC1)** Status Registers	Port 3B **(SFP)** Status Registers
64-77	0x40-0x4D	Port 4A Control Registers	Port 4B **(DSL DC)** Control Registers
78-79	0x4E-0x4F	Port 4A Status Registers	Port 4B **(DSL DC)** Status Registers
80-93	0x50-0x5D	Port 5A **(uC DIAG / MII)** Control Registers	Port 5B (SWB-SWA) Control Registers
94-95	0x5E-0x5F	Port 5A **(uC DIAG / MII)** Status Registers	Port 5B (SWB-SWA) Status Registers
96-103	0x60-0x67	TOS Priority Control Registers	
104-109	0x68-0x6D	MAC Address Registers	
110-111	0x6E-0x6F	Indirect Access Control Registers	
112-120	0x70-0x78	Indirect Data Registers	

*Refer to Micrel datasheet KSZ8895FQXIA for more detailed register description.

The Ethernet switch registers described in the table above can be accessed via Modbus registers 40100-40227 (switch A) and 40228-40355 (switch B). See section 10.0 for more details.

8.0 Telnet Interface (uC DIAG Only)

The 922-DSLH card implements a Telnet server on port 23. The server can be accessed from a PC-based Telnet client such as Microsoft Telnet Client™ or Tera Term by entering the card's IP address. Once a connection has been established, the Telnet interface displays a home screen containing a list of the available commands and also detailed help on using each command.

Typically the Telnet interface is used for convenient configuration of the TCP/IP settings of the card.
The commands available in the Telnet interface are shown in the figure below; detailed help for each command is available from the Telnet menu.

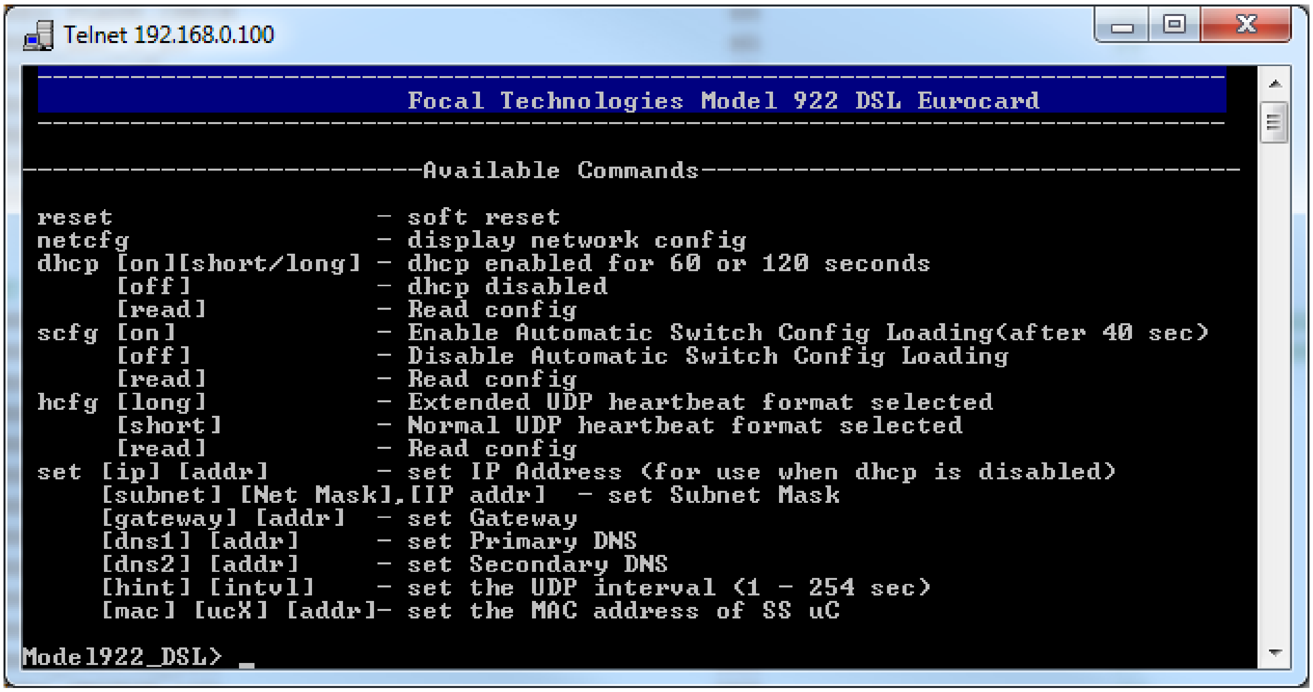

Figure 8-1: Telnet Interface

Telnet Session Negotiation

Normally, when a PC-based Telnet client such Microsoft Telnet Client™ or Tera Term is used to open a session with the 922 card's Telnet server, the Telnet client automatically responds to the server's negotiation options without further user interaction and a Telnet session can be open without problems.

For cases in which a PC-based Telnet client is not used, the user must ensure that the client responds to the server's negotiation options. The table below shows the typical negotiation options offered by the card's Telnet server and the responses that the client should provide in order to open a session.

Table 8-1: Telnet Negotiation Example

Source	IAC	Command	Sub cmd Option	Notes
Card Server	0xFF	0xFD	0x03	Do Suppress Go Ahead
	0xFF	0xFE	0x01	Don't Echo
	0xFF	0xFB	0x01	Will Echo
Client	0xFF	0xFB	0x03	Will Suppress Go Ahead
	0xFF	0xFC	0x01	Won't Echo
	0xFF	0xFD	0x01	Do Echo

`Client data in a single Ethernet frame → FF FB 03 FF FC 01 FF FD 01 = Will - Suppress Go Ahead, Won't - Echo, Do - Echo`

Note that the client responses do not necessarily need to be in the same Ethernet frame, but this is recommended. Once a Telnet session is open, there must be a carriage return (0x0D) followed by a line feed (0x0A) after every Telnet command send by the client.

The following table provides examples of the Telnet commands.

Table 8-2: Telnet Commands

<table>
<tr><th>Command</th><th>Description</th><th>Example</th></tr>
<tr><td>netcfg</td><td>Displays current network configuration. If the network configuration has been changed, netcfg will also show the settings to be applied on reset.</td><td>Input: netcfg

Telnet Output:
<pre>
Model922_DSL> netcfg
     DHCP: Disabled
      MAC: 00-09-CC-08-13-03
       IP: 192.168.0.100
   Subnet: 255.255.255.0
  Gateway: 192.168.0.1
     DNS1: 8.8.8.8
     DNS2: 8.8.4.4
</pre></td></tr>
<tr><td>dhcp [on/off] [short/long]</td><td>Enables or disables DHCP and sets the timeout length. For more information see section 0.</td><td>Input: dhcp on long
dhcp on short

Telnet Output:
<pre>
Model922_DSL> dhcp on long
DHCP Enabled for 120 seconds at startup
--> send 'reset' cmd to activate new setting...

Model922_DSL> dhcp on short
DHCP Enabled for 60 seconds at startup
--> send 'reset' cmd to activate new setting...

Model922_DSL> dhcp off
--> Saved DHCP disable to EEPROM
--> send 'reset' cmd to activate new setting...
</pre></td></tr>
<tr><td>scfg [on/off]</td><td>Enables or disables automatic switch configuration loading. This will load the switch configuration stored in EEPROM 40 seconds (approx.) after a power up. For more information see section 9.6.</td><td>Input: scfg on

Telnet Output:
<pre>
Model922_DSL> scfg on
!!!!!!!!!!!!!!!!!!!!!!!!!!Warning!!!!!!!!!!!!!!!!!!!!!!!!!!
Changing Ethernet Switch Configuration Autoload settings could
render the card inaccessible
Please ensure that a valid configuration is stored in the EEPROM
before enabling the Auto Load Feature
Do you still want to change it ? Yes\NO
</pre></td></tr>
<tr><td>hcfg [long/short]</td><td>Configures the UDP heartbeat packet to normal or extended format.</td><td>Input: hcfg long

Telnet Output:
<pre>
Model922_DSL> hcfg long
Extended UDP heartbeat packet enbled.....

Model922_DSL> hcfg short
Normal UDP heartbeat packet enbled.....
</pre></td></tr>
</table>

Command	Description	Example

set ip [addr]	Sets a new IP address. This action is protected by IP validation. For more information see section 9.10.	**Input:** set ip 192.168.0.100
		
		Telnet Output:
		`Model922_DSL> set ip 192.168.0.100`
		`--> Updating IP Address... success`
		`--> send 'reset' cmd to activate new settings...`

set subnet [netmask], [ip addr]	Sets a new subnet mask. This action is protected by Subnet validation. For more information see section 9.10.	**Input:** set subnet 255.255.255.0,192.168.0.100
		
		Telnet Output:
		`Model922_DSL> set subnet 255.255.255.0,192.168.0.100`
		`success IP Addres and Subnet Mask Updated`
		`--> send 'reset' cmd to activate new settings...`

set gateway [addr]	Sets the gateway.	**Input:** set gateway 192.168.0.1
		
		Telnet Output:
		`Model922_DSL> set gateway 192.168.0.1`
		`--> Updating Gateway... success`
		`--> send 'reset' cmd to activate new settings...`

set dns1/dns2 [addr]	Sets the primary (dns1) or secondary (dns2) DNS.	**Input:** set dns1 8.8.8.8
		
		Telnet Output:
		`Model922_DSL> set dns1 8.8.8.8`
		`--> Updating Primary DNS... success`
		`--> send 'reset' cmd to activate new settings...`

set hint [intvl]	Sets the UDP heartbeat interval. Valid inputs are 1-254 secs. For more information see section 0.	**Input:** set hint 30
		
		Telnet Output:
		`Model922_DSL> set hint 30`
		`--> UDP Heartbeat Interval... success`
		`--> UDP Heartbeat Interval set to 30 (sec)...`

9.0 Special Features

The 922-DSLH has several special features to support subsea applications:

- Remote Firmware Upgrade
- Loading and Saving User Switch Configuration
- DHCP Enable/Disable with timeouts
- Software Reset
- Watchdog Reset
- Automatic User Switch Configuration Loading
- UDP Heartbeat with critical card status
- Multiple Modbus Clients
- MIB Counters
- IP Validation

9.1 Remote Firmware Upgrade

The 922-DSLH card allows users to update the application firmware for the board's microcontroller over a TCP/IP interface using a proprietary protocol with multiple verification stages. Focal provides the necessary software and instructions for performing infield firmware upgrades. Please refer to the **Focal 922-0604-00 922 Remote Firmware Upgrade Guide** for detailed information on performing remote firmware upgrades to the cards.

After the Firmware update of the microcontroller is completed the 922-DSLH card will automatically reset twice before finalizing the update. In case of a failure during a firmware update the 922-DSLH card will automatically load the factory default application firmware.

9.2 Loading and Saving Switch Configuration

The 922-DSLH card allows the users to load and save Ethernet switch configuration from/into an EEPROM.

The current Ethernet switch configuration can be saved as a group to the EEPROM by writing 0x0001 to Modbus register 40380. A saved USER Ethernet switch configuration from EEPROM can be loaded into the switch by writing 0x0002 to Modbus register 40380. The user can revert back to the factory default Ethernet switch settings by writing 0x0004 to Modbus register 40380.

To change the registers of Ethernet switch A, write the switch register to be changed to Modbus register 40373 and the corresponding data to Modbus register 40374. Then write 1 to register 40375 for triggering a write to Ethernet switch A.

To change the registers of Ethernet switch B, write the switch register to be changed to Modbus register 40376 and the corresponding data to Modbus register 40377. Then write 1 to register 40378 for triggering a write to Ethernet switch B.

9.3 DHCP Enable/Disable

The 922-DSLH uC DIAG can obtain its IP address by using the Dynamic Host Configuration Protocol (DHCP). This feature can be enabled or disabled through the Telnet interface.

If this feature is enabled, then on power up the card sends a DHCP query and waits up to the duration of the DHCP timeout for a valid response. On receipt of a valid response from a DHCP server, the address specified by the DHCP response is used as the IP address.

If the card fails to receive a valid DHCP response within the configured timeout period, then the static IP address saved in the EEPROM is used as the IP address. If the EEPROM access were to fail, the card uses the address 192.168.0.100 as its IP address. **It is important to note that by default the DHCP functionality is enabled and the DHCP timeout is 60 seconds.**
DHCP is enabled by sending one of the following commands through the Telnet interface, “dhcp on short” or “dhcp on long”. These commands will enable DHCP with a timeout of 60 or 120 seconds respectively. DHCP is disabled by sending “dhcp off”.

9.4 Software Reset

A soft reset can be applied to the 922-DSLH card by sending the reset command from the Telnet menu.

Note that any changes to the Ethernet switch configuration made prior to the reset will be lost and the Ethernet switch will start up with the default Ethernet switch configuration.

9.5 Watchdog Reset

The 922-DSLH card has a built in watchdog timer which is used by the processor to trigger a watchdog reset in case of a software lock up. The exact timing parameters of the watchdog reset are beyond the scope of this document.

9.6 Automatic User Switch Configuration Loading

The 922-DSLH can automatically load the user-defined Ethernet switch configuration already saved in EEPROM. This functionality can be enabled or disabled through the Telnet interface by sending a “scfg on” or “scfg off” command. If this feature is enabled, then on power-up the card loads the “User Ethernet Switch Configuration” from the EEPROM after ~40 seconds.

Note that this feature is disabled by default and the user has to make sure that they save a valid copy of the switch configuration in the EEPROM before enabling this functionality. Failure to do so may result in loss of connectivity to the card.

9.7 UDP Heartbeat Packet

922-DSLH cards will continuously transmit a broadcast heartbeat User Datagram Packet (UDP) from the microcontroller with diagnostics information after power-up. The card transmits this packet every five (5) seconds by default. This interval can be adjusted to any value between 1 and 254 seconds through Telnet. The data is printed out as comma separated text (ASCII) and a network capture utility (e.g. Wireshark) can be used to capture this data. The UDP heartbeat can be used, for example, to identify cards in cases where the IP information has been lost.

The 922-DSLH card can output the UDP heartbeat in two different packet lengths: short (normal) and extended. The “short” packet contains the following diagnostics information:

- Serial number, date code, assembly number and firmware version
- MAC address, IP address, subnet, gateway, primary and secondary DNS

The “extended” packet includes all the information from the short packet plus the following diagnostics information:

- Card on time, number of off events, card temperature, card voltage, current draw
- Link status of copper ports CU1 and CU2

The 922-DSLH cards output the “short” packet version by default. The table below shows an example of the diagnostics information contained in each type of UDP heartbeat packet. The heartbeat packet type can be changed through Telnet by sending the command “hcfg long” for extended packets or “hcfg short” for short packets.

Table 9-1: Model 922 UDP Heartbeat Packet Content (From uC DIAG)

UDP Heartbeat Packet Example	
“Short” Packet (default)	**“Extended” Packet**
Serial No : 10054378******** Date Code : 20170511******** Assembly No : 922-5016-00***** FW VER : A3 MAC ADDRESS : 00-09-CC-08-12-A7 LOCAL IP : 192.168.0.100 Subnet : 255.255.255.0 Gateway : 192.168.0.1 Prim DNS : 8.8.8.8 Sec DNS : 8.8.4.4	Model 922 Dual DSL Carrier Card Information Serial No : 10054378******** Date Code : 20170511******** Assembly No : 922-5016-00***** FW VER : A3 MAC ADDRESS : 00-09-CC-08-12-A7 LOCAL IP : 192.168.0.100 Subnet : 255.255.255.0 Gateway : 192.168.0.1 Prim DNS : 8.8.8.8 Sec DNS : 8.8.4.4 ON Time : 24 Days 0 Hours Number of OFF Events : 247 Board Temperature(degC) : 0.00 +5V Supply : 4.942 Board Current(A) : 0.27 CU 1 Link : Linked CU 2 Link : Not Linked

9.8 Multiple Modbus Clients

922-DSLH cards provide support for up to four (4) Modbus clients. This feature allows the user to establish more than one Modbus TCP/IP connection (up to 4) to the same card. When more than one connection is established to the card, some packet collisions and re-transmission are expected. In general, when using multiple TCP connections to the same card, it is recommended to set the Modbus poll rate to a value greater than 1 second.

9.9 Management Information Base (MIB) Counters

The onboard Micrel switch provides access to the MIB counters on 922-DSLH card. The counters can be viewed using the Focal diagnostic software, as seen in the figure below, or by reading Modbus registers 40401-41050 as outlined in section 0.

The Focal diagnostic software provides both a summarized history of the counters and the active values, which are sampled every half second. The port usage meters represent the amount of traffic on a port in either direction (transmit or receive with respect to the card). Alarm indicators will show and highlight any active or past errors.

The following figure shows the “History” view of the P1 SwA MIB counters. The “History” view displays the software-accumulated counts since the last time a GUI connection was established with the card. If the GUI is re-started or closed then the history of counts will be cleared.

Figure 9-1: MIB Counters

The “Active” view displays the live counts measured by the switch/microcontroller in the last half a second. This refresh interval is fixed in hardware and cannot be changed via the GUI.

The “Clear” button is only visible when the user selects the “History” view. When the user presses the “Clear” button, the total “History” of error counts is set to 0. Switching between “Active” and “History” views does not clear any accumulated counts.

The following figure shows the alarm indicators for a connection with collision errors on P2 of switch A (CU1). The top left red error LED indicator only appears when one (1) or more errors are detected in any of the Ethernet ports. In the example below, only P2 is reporting errors. Note that red LEDs indicate one (1) or more errors and green LEDs indicate no errors (i.e. 0 errors).

Figure 9-2: MIB Counters With Error Indicators

For descriptions of the various MIB counters refer to the switch data sheet for KSZ8895FQXIA.

9.10 IP Settings for Diagnostics (uC DIAG)

922-DSLH cards include an IP validation feature in the Telnet interface. This feature checks for a valid IP and subnet combination. If an invalid IP Address is entered using the “set ip” command, the Telnet interface will show the user the valid range of IP addresses within the current subnet. Additionally, subnet validation will ensure that the user is providing a valid subnet when using the “set subnet” command. Examples of an invalid IP entry, a valid IP entry and an invalid subnet entry can be seen in the figures below.

IP validation also occurs during the startup procedure. If on startup an invalid IP address or subnet is read from the EEPROM, these parameters will be set to the factory defaults.

```
Model922_DSL> set ip 0.0.0.0
--> Invalid IP Address specified for the Subnet...
Entered IP     = 0.0.0.0
Saved Net Mask = 255.255.255.0

Following addresses cannot be used as host IP
Subnet Base      = 192.168.0.0
Subnet Broadcast = 192.168.0.255

Allowed Host IP range
Subnet Host Min Addr  = 192.168.0.1
Subnet Host Max Addr  = 192.168.0.254
```

Figure 9-3: Telnet Invalid IP Entry

```
Model922_DSL> set ip 192.168.0.100
--> Updating IP Address... success
--> send 'reset' cmd to activate new settings...
```

Figure 9-4: Valid IP Entry

```
Model922_DSL> set subnet 0.0.0.0,192.168.0.100
--> Invalid Subnet Mask IP specified...
```

Figure 9-5: Invalid Subnet Entry

10.0 Modbus Register Maps

Board Info Registers				
Register Number	**Bit**	**R/W**	**Description**	**Comments**
40001 - 40008	[15:0]	R	Board Serial Number	
40009 - 40016	[15:0]	R	Board Date Code	
40017 - 40024	[15:0]	R	Board Assembly Number	
40025 - 40032	[15:0]	R	Reserved	
40033 - 40040	[15:0]	R	Board MAC Address	
40041 - 40048	[15:0]	R	Board IP Address	
40049	[15:0]	R	Reserved	
40050	[15:0]	R	Board Current	Current = value * 0.001953125
40051	[15:0]	R	Board 3.3V Voltage	Voltage = value * 0.005859375
40052	[15:0]	R	Reserved	
40053	[15:0]	R	Board Humidity	Humidity = (value * 0.0019073) - 6
40054	[15:0]	R	Board Temperature	Temperature = (value * 0.0026812) – 46.5
40055	[15:8]	R	Diagnostic uC FW Load Location	0-uC Internal Flash 1-User Flash 2-Factory Flash
	[7:0]	R	Diagnostic uC FW Revision	
40056	[15:0]	R	Cause of Last uC Reset	0-Power Up 2-Watchdog 3-Software 4-User (NRST pin) 5-Brownout
40057	[15:0]	R	Elapsed ON Time (Lower 16-bits)	The time from first power up in 0.25 second increments (lower 16 bits)
40058	[15:0]	R	Elapsed ON Time (Upper 16-bits)	The time from first power up in 0.25 second increments (upper 16 bits)
40059	[15:0]	R	OFF Event Counter	Incremented every time the power to the card is turned OFF
40060	[15:0]	R	I2C Error Counter	
40061	[15:0]	R	SPI Error Counter	
40062	[15:7]	R	Reserved	
	7	R	UVLAN1 Status	1- User VLAN 1 Enabled 0- User VLAN 1 Disabled
	5	R	HCFG Status	1- Long message format 0- Short message format
	4	R	SCFG Status	1- Switch Config form EEPROM Enabled 0- Switch Config from EEPROM Disabled
	3	R	LCFG Status	1- Front Panel LED Board Enabled 0- Front Panel LED Board Disabled
	2	R	Reserved	
	1	R	DHCP Interval	1- Long (120 sec) 0- Short (60 sec)
	0	R	DHCP Status	1- DHCP Enabled 0- DHCP Disabled
40063	[15:14]	R	Reserved	
	[13]	R	SS2 Rx Active	
	[12]	R	SS2 Tx Active	
	[11:10]	R	Reserved	
	[9]	R	SS1 Rx Active	
	[8]	R	SS1 Tx Active	
	[7:0]	R	Reserved	

Board Info Registers				
Register Number	**Bit**	**R/W**	**Description**	**Comments**
40064	[15:6]	R	Reserved	
	[5:4]	R	User Flash Status	1- Failed 2- OK
	[3:2]	R	Factory Flash Status	1- Failed 2- OK
	[1:0]	R	Internal Flash Status	1- Failed 2- OK
40065	[15:0]	R	Board 1.2V Voltage	Voltage = value * 0.0029296875
40066	[15:0]	R	Board 5.0V Voltage	Voltage = value * 0.005859375
40067	[15:0]	R	Reserved	
40068	[15:0]	R	DC2 UART Error Count	Error count for daughter card slot 2 (DSL1)
40069	[15:0]	R	SS1 UART Error Count	Internal communication error counter for SS1
40070	[15:0]	R	SS2 UART Error Count	Internal communication error counter for SS2
40071-40099	[15:0]	R	Reserved	

Ethernet Status Registers				
Register Number	**Bit**	**R/W**	**Description**	**Comments**
40100-40227	[15:0]	R	Switch A Register Map	Refer to Micrel datasheet KSZ8895FQXIA for more detailed register description.
40228-40355	[15:0]	R	Switch B Register Map	
40356-40369	[15:0]	R	Reserved	
40370	[15:10]	R	Reserved	
	9	R	SWB-SWA Link Status	1 – Linked 0 – No Link
	8	R	DSL Ethernet Link Status	
	7	R	SFP Internal Link Status	
	6	R	CU2 Link Status	
	5	R	SS2 Ethernet Link Status	
	4	R	uC Ethernet Link Status	
	3	R	SwA P4 Ethernet Link Status	
	2	R	SS1 Ethernet Link Status	
	1	R	CU1 Link Status	
	0	R	SWA-SWB Link Status	
40371	[15:10]	R	Reserved	
	9	R	SWB-SWA Link Speed	1 – 100 Base-Tx 0 – 10 Base-T
	8	R	DSL Ethernet Link Speed	
	7	R	SFP Internal Link Speed	
	6	R	CU2 Link Speed	
	5	R	SS2 Ethernet Link Speed	
	4	R	uC Ethernet Link Speed	
	3	R	SwA P4 Ethernet Link Speed	
	2	R	SS1 Ethernet Link Speed	
	1	R	CU1 Link Speed	
	0	R	SWA-SWB Link Speed	
40372	[15:10]	R	Reserved	
	9	R	SWB-SWA Link Duplex	1 – Full Duplex 0 – Half Duplex
	8	R	DSL Ethernet Link Duplex	
	7	R	SFP Internal Link Duplex	
	6	R	CU2 Link Duplex	
	5	R	SS2 Ethernet Link Duplex	

Ethernet Status Registers				
Register Number	**Bit**	**R/W**	**Description**	**Comments**
	4	R	uC Ethernet Link Duplex	
	3	R	SwA P4 Ethernet Link Duplex	
	2	R	SS1 Ethernet Link Duplex	
	1	R	CU1 Link Duplex	
	0	R	SWA-SWB Link Duplex	
40373	[15:0]	R/W	Ethernet Switch A Write Address	This register holds a switch register address. (Only lower 8 bits used)
40374	[15:0]	R/W	Ethernet Switch A Write Data	This register holds a switch register data. (Only lower 8 bits used)
40375	[15:3]	R/W	Ethernet Switch A Write Trigger	Reserved
	2	R/W	Ethernet Switch A Write Confirm	Triggers uC DIAG to confirm that loading a new switch A configuration is allowed. Set this bit after Ethernet Switch A Trigger Write is completed.
	1	R/W	Ethernet Switch A Trigger Read	Triggers uC DIAG to read the current switch configuration and save the result in Ethernet Switch A registers.
	0	R/W	Ethernet Switch A Trigger Write	Triggers uC DIAG to write data from 40374 into the address in 40373. The uC resets this bit to 0 after the write is completed.
40376	[15:0]	R/W	Ethernet Switch B Write Address	This register holds a switch register address. (Only lower 8 bits used)
40377	[15:0]	R/W	Ethernet Switch B Write Data	This register holds a switch register data. (Only lower 8 bits used)
40378	[15:3]	R/W	Ethernet Switch B Write Trigger	Reserved
	2	R/W	Ethernet Switch B Write Confirm	Triggers uC DIAG to confirm that loading a new switch B configuration is allowed. Set this bit after Ethernet Switch B Trigger Write is completed.
	1	R/W	Ethernet Switch B Trigger Read	Triggers uC DIAG to read the current switch configuration and save the result in Ethernet Switch A registers.
	0	R/W	Ethernet Switch B Trigger Write	Triggers uC DIAG to write data from 40377 into the address in 40376. The uC resets this bit to 0 after the write is completed.
40379	[15:0]	R	Reserved	
40380	[15:3]	R/W	Ethernet Switch Control Register	Reserved
	2	R/W	Load Default Ethernet Switch Configuration (Bootstrap)	Triggers the uC to restart the switch in boot strap mode. The uC resets this bit to 0 after the restart is complete.
	1	R/W	Load User Ethernet Switch Configuration from EEPROM	Triggers the uC to restart the switch in user settings mode. The uC resets this bit to 0 after restart is complete.
	0	R/W	Save Current Ethernet Switch Config to EEPROM	Triggers the uC to write all config registers to EEPROM. The uC resets this bit to 0 after EEPROM write is complete.
40381	[15:0]	R	Reserved	
40382	[15:0]	R	Ethernet Switch Cu1 Control [0x2C,0x2E] SwA	See KSZ8895FQXIA
40383	[15:0]	R	Ethernet Switch Cu2 Control [0x2C,0x2E] SwB	See KSZ8895FQXIA
40384-40400	[15:0]	R	Reserved	
40401-40465	[15:0]	R	SA_P1 MIB Counters	See MIB Counters section
40466-40530	[15:0]	R	SA_P2 MIB Counters	
40531-40595	[15:0]	R	SA_P3 MIB Counters	
40596-40660	[15:0]	R	SA_P4 MIB Counters	
40661-40725	[15:0]	R	SA_P5 MIB Counters	
40726-40790	[15:0]	R	SB_P1 MIB Counters	

Ethernet Status Registers				
Register Number	**Bit**	**R/W**	**Description**	**Comments**
40791-40855	[15:0]	R	SB_P2 MIB Counters	
40856-40920	[15:0]	R	SB_P3 MIB Counters	
40921-4985	[15:0]	R	SB_P4 MIB Counters	
40986-41050	[15:0]	R	SB_P5 MIB Counters	
41051-41145	[15:0]	R	Reserved	

FW Update Registers				
Register Number	**Bit**	**R/W**	**Description**	**Comments**
41146	[15:0]	R/W	Reserved	
41147	[15:0]	R/W	FW Update File Size (Upper 8-bits)	
41148	[15:0]	R/W	FW Update File Size (Middle 8-bits)	
41149	[15:0]	R/W	FW Update File Size (Lower 8-bits)	
41150	[15:0]	R/W	FW Update Ready To Load or Done	
41151	[15:0]	R/W	Page Ready/Done	
41152	[15:0]	R/W	FW Update Finalization	
41153-41166	[15:0]	R/W	FW Update Control Reserved	
41167-41422	[15:0]	R/W	FW Registers	
41423-41499	[15:0]	R/W	FW Registers Reserved	

SERIAL SERVER CH1 AND CH2 MODBUS REGISTERS

SS1,2 Registers				
Register Number	**Bit**	**R/W**	**Description**	**Comments**
41500-42523	[15:0]	R/W	Reserved	
42524-42779	[15:0]	R/W	SS1 EEPROM Registers	For EEPROM registers see section 0 For general purpose (GP) registers see section 0
42780-43035	[15:0]	R	SS1 GP Registers	
43036-43291	[15:0]	R/W	SS2 EEPROM Registers	
43292-43547	[15:0]	R	SS2 GP Registers	

SS1,2 Indirect Access Registers				
Register Number	**Bit**	**R/W**	**Description**	**Comments**
43548	[15:0]	R/W	uC ID	Set to 3 or 4 to select target uC 1 or 2 respectively
43549	[15:0]	R/W	uC Data Start Address	
43550-44061	[15:0]	R/W	uC Data	
44062	[15:0]	R/W	uC Number of Bytes	
44063	[15:0]	R/W	uC Operation	0x01-Reset uC, 0x02-Write Data to EEPROM, 0x03-Write Data to uC GP Registers, 0x04-Command Failed Flag. This register will is self-clearing to 0x00. If command failed will return 0x04.

DSL MODBUS RESISTERS

DSL Registers				
Register Number	**Bit**	**R/W**	**Description**	**Comments**
41500-44064	[15:0]	R	Reserved	
44065	[15:0]	R	DSL1 Linestate	0x00 – Down Read 0x01 – Initializing 0x02 – Up Data Mode 0x03 – Stop Down Ready 0x04 – Down Not Ready 0xFF – Unknown
44066	[15:0]	R	DSL1 Mode	0x00 – STU-R (CPE) 0x01 – STU-C (CO) 0xFF – Unknown
44067	[15:0]	R	DSL1 Bitrate	Bitrate in kbps
44068	[15:0]	R	DSL1 PAM	TC-PAM
44069	[15:0]	R	DSL1 SNRM	DSL Signal Noise Ratio Margin (dB)
44070	[15:0]	R	DSL1 LATN	DSL Line Attenuation (dB)
44071	[15:0]	R	DSL1 Is Auto	0x00 – Bitrate is fixed 0x01 – Bitrate is set to auto
44072	[15:0]	R	DSL1 Ratemode	0x01 – gshdsl 0x02 – gshdsl.bis 0x03 – extended 0xFF – Unknown
44073-44127	[15:0]	R	Reserved	

DSL Command Interface Registers				
Register Number	**Bit**	**R/W**	**Description**	**Comments**
44128	[15:0]	R	DSL DC Channel	0x02 – DSL1
44129	[15:0]	R	DSL Command ID	See DSL Command List
44130	[15:0]	R	DSL Command Trigger	To trigger a DSL command write 0x01 to this register. Then poll this register for the response code. 0x00 – Command succeeded 0x02 – Invalid device id 0x03 – Invalid command id 0x04 – Command Failed
44131	[15:0]	R	DSL Command Argument 0	See DSL Command List
44132	[15:0]	R	DSL Command Argument 1	
44133	[15:0]	R	DSL Command Argument 2	
44134	[15:0]	R	DSL Command Argument 3	
44135	[15:0]	R	DSL Command Argument 4	

10.1 DSL Command List

Command ID 0x05: Set temporary DSL settings

Arguments:

0 – DSL Mode	(0x00 – STU-R (CPE), 0x01 – STU-C (CO))
1 – DSL Bitrate	(Bitrate in kbps)
2 – DSL PAM	(TC-PAM)
3 – DSL Ratemode	(0x00 – g.shdsl, 0x01 – g.shdsl.bis, 0x02 – extended)

Example: The example shows the command for setting DSL1 as STU-C, 192kbps, 4 TC-PAM, extended mode

Write Reg[44128] = 0x02 //Select DSL1
Write Reg[44129] = 0x05 //Set command ID 0x05
Write Reg[44131] = 0x01 //Select STU-C
Write Reg[44132] = 0xC0 //Select bitrate 192kbps
Write Reg[44133] = 0x04 //Select PAM 4
Write Reg[44134] = 0x02 //Select Ratemode extended
Write Reg[44130] = 0x01 //Trigger write

Read Reg[44130] = 0x00 //Command Succeeded

10.2 MIB Counters

MIB Counters (see Micrel datasheet KSZ8895FQXIA for more information)				
Offset	**Bit**	**R/W**	**Name**	**Description**
0	[15:0]	R	RxLoPriorityByte [LSB]	Rx low-priority (default) octet count including bad packets.
1	[15:0]	R	RxLoPriorityByte [MSB]	
2	[15:0]	R	RxHiPriorityByte [LSB]	Rx high-priority octet count including bad packets.
3	[15:0]	R	RxHiPriorityByte [MSB]	
4	[15:0]	R	RxUndersizePkt [LSB]	Rx undersized packets with good CRC.
5	[15:0]	R	RxUndersizePkt [MSB]	
6	[15:0]	R	RxFragments [LSB]	Rx fragment packets with bad CRC, symbol errors or alignment errors.
7	[15:0]	R	RxFragments [MSB]	
8	[15:0]	R	RxOversize [LSB]	Rx oversize packets with good CRC.
9	[15:0]	R	RxOversize [MSB]	
10	[15:0]	R	RxJabbers [LSB]	Rx packets longer than 1522B with either CRC errors, alignment errors, or symbol errors (depends on max packet size setting) or Rx packets longer than 1916B only.
11	[15:0]	R	RxJabbers [MSB]	
12	[15:0]	R	RxSymbolError [LSB]	Rx packets with invalid data symbol and legal preamble, packet size.
13	[15:0]	R	RxSymbolError [MSB]	
14	[15:0]	R	RxCRCError [LSB]	Rx packets within (64, 1522) bytes with an integral number of bytes and a bad CRC (upper limit depends on max packet size setting).
15	[15:0]	R	RxCRCError [MSB]	
16	[15:0]	R	RxAlignmentError [LSB]	Rx packets within (64, 1522) bytes with a non-integral number of bytes and a bad CRC (upper limit depends on max packet size setting).
17	[15:0]	R	RxAlignmentError [MSB]	
18	[15:0]	R	RxControl8808Pkts [LSB]	The number of MAC control frames received by a port with 88-08h in EtherType field.
19	[15:0]	R	RxControl8808Pkts [MSB]	
20	[15:0]	R	RxPausePkts [LSB]	The number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and valid CRC.
21	[15:0]	R	RxPausePkts [MSB]	
22	[15:0]	R	RxBroadcast [LSB]	Rx good broadcast packets (not including erred broadcast packets or valid multicast packets).
23	[15:0]	R	RxBroadcast [MSB]	
24	[15:0]	R	RxMulticast [LSB]	Rx good multicast packets (not including MAC control frames, erred multicast packets or valid broadcast packets).
25	[15:0]	R	RxMulticast [MSB]	
26	[15:0]	R	RxUnicast [LSB]	Rx good unicast packets.
27	[15:0]	R	RxUnicast [MSB]	
28	[15:0]	R	Rx64Octets [LSB]	Total Rx packets (bad packets included) that were 64 octets in length.
29	[15:0]	R	Rx64Octets [MSB]	
30	[15:0]	R	Rx65To127Octets [LSB]	Total Rx packets (bad packets included) that are between 65 and 127 octets in length.
31	[15:0]	R	Rx65To127Octets [MSB]	
32	[15:0]	R	Rx128To255Octets [LSB]	Total Rx packets (bad packets included) that are between 128 and 255 octets in length.
33	[15:0]	R	Rx128To255Octets [MSB]	
34	[15:0]	R	Rx256To511Octets [LSB]	Total Rx packets (bad packets included) that are between 256 and 511 octets in length.
35	[15:0]	R	Rx256To511Octets [MSB]	
36	[15:0]	R	Rx512To1023Octets [LSB]	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length.
37	[15:0]	R	Rx512To1023Octets [MSB]	
38	[15:0]	R	Rx1024To1522Octets [LSB]	Total Rx packets (bad packets included) that are between 1024 and 1522 octets in length (upper limit depends on max packet size setting).
39	[15:0]	R	Rx1024To1522Octets [MSB]	
40	[15:0]	R	TxLoPriorityByte [LSB]	Tx low-priority good octet count, including PAUSE packets.
41	[15:0]	R	TxLoPriorityByte [MSB]	
42	[15:0]	R	TxHiPriorityByte [LSB]	Tx high-priority good octet count, including PAUSE packets.
43	[15:0]	R	TxHiPriorityByte [MSB]	
44	[15:0]	R	TxLateCollision [LSB]	

MIB Counters (see Micrel datasheet KSZ8895FQXIA for more information)				
Offset	**Bit**	**R/W**	**Name**	**Description**
45	[15:0]	R	TxLateCollision [MSB]	The number of times a collision is detected later than 512 bit-times into the Tx of a packet.
46	[15:0]	R	Tx PausePkts [LSB]	The number of PAUSE frames transmitted by a port.
47	[15:0]	R	Tx PausePkts [MSB]	
48	[15:0]	R	TxBroadcastPkts [LSB]	Tx good broadcast packets (not including erred broadcast or valid multicast packets).
49	[15:0]	R	TxBroadcastPkts [MSB]	
50	[15:0]	R	TxMulticastPkts [LSB]	Tx good multicast packets (not including erred multicast packets or valid broadcast packets).
51	[15:0]	R	TxMulticastPkts [MSB]	
52	[15:0]	R	TxUnicastPkts [LSB]	Tx good unicast packets.
53	[15:0]	R	TxUnicastPkts [MSB]	
54	[15:0]	R	TxDeferred [LSB]	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium.
55	[15:0]	R	TxDeferred [MSB]	
56	[15:0]	R	TxTotalCollision [LSB]	Tx total collision, half duplex only.
57	[15:0]	R	TxTotalCollision [MSB]	
58	[15:0]	R	TxExcessiveCollision [LSB]	A count of frames for which Tx fails due to excessive collisions.
59	[15:0]	R	TxExcessiveCollision [MSB]	
60	[15:0]	R	TxSingleCollision [LSB]	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision.
61	[15:0]	R	TxSingleCollision [MSB]	
62	[15:0]	R	TxMultipleCollision [LSB]	Successfully Tx frames on a port for which Tx is inhibited by more than one collision.
63	[15:0]	R	TxMultipleCollision [MSB]	

10.3 Serial Server EEPROM Registers

SS1,2 EEPROM Memory map				
Address	**Bit**	**Category**	**Description**	**Comments**
0	[7:0]	Ethernet	MAC [47:40]	
1	[7:0]		MAC [39:32]	
2	[7:0]		MAC [31:24]	
3	[7:0]		MAC [23:16]	
4	[7:0]		MAC [15:8]	
5	[7:0]		MAC [7:0]	
6-15	[7:0]		Reserved	
16	[7:0]		Gateway [7:0]	
17	[7:0]		Gateway [15:8]	
18	[7:0]		Gateway [23:16]	
19	[7:0]		Gateway [31:24]	
20	[7:0]		DNS [7:0]	
21	[7:0]		DNS [15:8]	
22	[7:0]		DNS [23:16]	
23	[7:0]		DNS [31:24]	
24	[7:0]		DNS [7:0]	
25	[7:0]		DNS [15:8]	
26	[7:0]		DNS [23:16]	
27	[7:0]		DNS [31:24]	
28	[7:0]		LAN Speed	0x00 = Auto 0x01 = 10Mbps 0x02 = 100Mbps
29	[7:0]		LAN Duplex	0x00 = Half 0x01 = Full
30-40	[7:0]		Reserved	
41	[7:0]		Local IP [7:0]	
42	[7:0]		Local IP [15:8]	
43	[7:0]		Local IP [23:16]	
44	[7:0]		Local IP [31:24]	
45	[7:0]		Local Netmask [7:0]	
46	[7:0]		Local Netmask [15:8]	
47	[7:0]		Local Netmask [23:16]	
48	[7:0]		Local Netmask [31:24]	
49-63	[7:0]		Reserved	
64	[7:0]	Serial Parameters	Baud [7:0]	
65	[7:0]		Baud [15:8]	
66	[7:0]		Baud [23:16]	
67	[7:0]		Baud [31:24]	
68	[7:0]		Data Bits	0x02 = 7 0x03 = 8
69	[7:0]		Stop Bits	0x00 = 1 0x01 = 1.5 0x02 = 2
70	[7:0]		Parity	0x00 = Even 0x01 = Odd 0x02 = Space 0x03 = Mark 0x04 = None
71	[7:0]		Flow Control	0x00 = None 0x01 = Software 0x02 = Hardware

SS1,2 EEPROM Memory map				
Address	**Bit**	**Category**	**Description**	**Comments**
72	[7:0]		Interface	0x00 = RS232 0x01 = RS485 0x02 = RS422
73	[7:0]		Termination	0x00 = Disabled 0x01 = Enabled
74-79	[7:0]		Reserved	
80	[7:0]	Operation	Operational Mode	0xFF = Disable 0x01 = UDP 0x02 = ModBus Gateway 0x03 = PPP
81-83	[7:0]		Reserved	
84	[7:0]	UDP Application	Local Listening Port [7:0]	
85	[7:0]		Local Listening Port [15:8]	
86	[7:0]		Destination IP [7:0]	
87	[7:0]		Destination IP [15:8]	
88	[7:0]		Destination IP [23:16]	
89	[7:0]		Destination IP [31:24]	
90	[7:0]		Destination Listening Port [7:0]	
91	[7:0]		Destination Listening Port [15:8]	
92	[7:0]		Inter-frame Delay [7:0]	
93	[7:0]		Inter-frame Daley [15:8]	
94-111	[7:0]		Reserved	
112	[7:0]	PPP Application	username char[0]	
113	[7:0]		username char[1]	
114	[7:0]		username char[2]	
115	[7:0]		username char[3]	
116	[7:0]		username char[4]	
117	[7:0]		username char[5]	
118	[7:0]		username char[6]	
119	[7:0]		username char[7]	
120	[7:0]		username char[8]	
121	[7:0]		password char[0]	
122	[7:0]		password char[1]	
123	[7:0]		password char[2]	
124	[7:0]		password char[3]	
125	[7:0]		password char[4]	
126	[7:0]		password char[5]	
127	[7:0]		password char[6]	
128	[7:0]		password char[7]	
129	[7:0]		password char[8]	
112	[7:0]		Password Enable	0x00 = Disabled 0x01 = Enabled
113	[7:0]		PPP Server IP [7:0]	
114	[7:0]		PPP Server IP [15:8]	
115	[7:0]		PPP Server IP [23:16]	
116	[7:0]		PPP Server IP [31:24]	
117	[7:0]		PPP Client IP [7:0]	
118	[7:0]		PPP Client IP [15:8]	
119	[7:0]		PPP Client IP [23:16]	
120	[7:0]		PPP Client IP [31:24]	
121	[7:0]		PPP Netmask [7:0]	

SS1,2 EEPROM Memory map				
Address	**Bit**	**Category**	**Description**	**Comments**
122	[7:0]		PPP Netmask [15:8]	
123	[7:0]		PPP Netmask [23:16]	
124	[7:0]		PPP Netmask [31:24]	
125	[7:0]		PPP Server/Client Mode	0x00 = Client 0x01 = Server
126-159	[7:0]		Reserved	
160	[7:0]	Modbus Application	Master/Slave Mode	0x00 = RTU Slave, 0x01 = RTU Master
161	[7:0]		Local Listening Port [7:0]	
162	[7:0]		Local Listening Port [15:8]	
163	[7:0]		Destination IP [7:0]	
164	[7:0]		Destination IP [15:8]	
165	[7:0]		Destination IP [23:16]	
166	[7:0]		Destination IP [31:24]	
167	[7:0]		Destination Listening Port [7:0]	
168	[7:0]		Destination Listening Port [15:8]	
169	[7:0]		Receive Timeout [7:0]	
170	[7:0]		Receive Timeout [15:8]	
171	[7:0]		Slave Response Timeout [7:0]	
172	[7:0]		Slave Response Timeout [15:8]	
173-254	[7:0]		Reserved	
255	[7:0]		Validation Byte	0x55 for EEPROM Valid

10.4 Serial Server General Purpose Registers

General Purpose Registers				
Offset	**Bit**	**R/W**	**Description**	**Comments**
0	[15:8]	R	Reserved	
	[7:4]	R	Running Code	1 = Bootloader 2 = Application Code
	[3:0]	R	Cause of Last Reset	0 = Power Up 2 = Watchdog 3 = Software 4 = User (NRST pin) 5 = Brownout
1	[15:8]	R	Reserved	
	[7:0]	R	FW Revision	
2	[15:0]	R	Tx Byte Count[3]	
3	[15:0]	R	Tx Byte Count[2]	
4	[15:0]	R	Tx Byte Count[1]	
5	[15:0]	R	Tx Byte Count[0]	
6	[15:0]	R	Rx Byte Count[3]	
7	[15:0]	R	Rx Byte Count[2]	
8	[15:0]	R	Rx Byte Count[1]	
9	[15:0]	R	Rx Byte Count[0]	
10-31	[15:0]	R	Reserved	
32	[15:0]	R	uC1 IP[3]	
33	[15:0]	R	uC1 IP[2]	
34	[15:0]	R	uC1 IP[1]	
35	[15:0]	R	uC1 IP[0]	
36	[15:0]	R	uC2 IP[3]	
37	[15:0]	R	uC2 IP[2]	
38	[15:0]	R	uC2 IP[1]	
39	[15:0]	R	uC2 IP[0]	
40	[15:0]	R	uC3 IP[3]	
41	[15:0]	R	uC3 IP[2]	
42	[15:0]	R	uC3 IP[1]	
43	[15:0]	R	uC3 IP[0]	
44	[15:0]	R	uC4 IP[3]	
45	[15:0]	R	uC4 IP[2]	
46	[15:0]	R	uC4 IP[1]	
47	[15:0]	R	uC4 IP[0]	
48-255	[15:0]	R	Reserved	